Large Angle Deviation in Grid-Following IBRs Upon Grid Voltage Dip

Lingling Fan, *Fellow, IEEE*, Zhengyu Wang, *Member, IEEE*, Zhixin Miao, *Senior Member, IEEE*

***Abstract*—In the 2021 Texas Odessa large-scale solar PV tripping events, phase-locked-loop (PLL) loss of synchronism is identified as a major cause of solar PV tripping. When solar PVs detected a large phase angle deviation (e.g., 10 degrees), tripping commands were initiated. The large phase angle deviation was triggered by a transmission line fault 200 miles away, which in turn led to approximately 30% voltage drop in the 345-kV system. This paper offers a plausible reason why grid-following inverter-based resources (IBRs) may experience a large angle deviation upon grid voltage dip. Critical operating conditions contributing to such phenomena are identified via analysis and their effects are demonstrated using electromagnetic transient (EMT) simulation. Furthermore, the effect of converter control, e.g., grid-following control vs. grid-forming control, is examined. It is found from EMT simulation results that frequency and voltage control are helpful in mitigating angle deviation. Furthermore, linear block diagrams are derived to examine why frequency control can effectively suppress large angle deviation.**

***Index Terms*—Solar photovoltaic, phase-locked loop, grid-following control, grid-forming control.**

I. Introduction

IN the 2021 Texas Odessa events [1], some solar PVs tripped when the phase angle deviation was beyond 10 degrees. According to [1], one of these solar PVs was the furthest plant from the fault, about 200 miles away. The fault caused the 345-kV transmission system experiencing about 30% voltage drop.

Below are the quotes from [1]: "*PLL Loss of Synchronism (389 MW): PLL loss of synchronism was the largest contributor to the reduction of solar PV output in this event. Two large BES facilities reduced output by 239 MW and 150 MW. This cause of tripping is specifically attributable to one inverter manufacturer and has been identified in multiple prior events analyzed by NERC. It is a systemic concern for facilities with this inverter type. Existing facilities are likely set with inverters that will trip when their voltage phase angle experiences a shift during fault events (i.e., 10 degree vector shift); the inverters issue a fault code and shut down.*"

The majority of the literature shows that PLL loss of synchronism occurs when a deep voltage dip is experienced by IBRs and/or the inverter's fault ride through logic takes effect to inject reactive power, e.g., [2]–[5]. Apparently, the assumed grid condition is far different from that of the Odessa events. In the Odessa events, the tripped solar PVs experienced about 30% voltage dip.

This project is supported in part by the US Department of Energy Solar Energy Technology Office DE-EE-0008771. L. Fan and Z. Miao are with the Department of Electrical Engineering, University of South Florida, Tampa, FL, 33620 (e-mail: linglingfan, zmiao@usf.edu). Z. Wang is with RWE Clean Energy, Austin TX, 78724 (email: zhengyu.wang@rwe.com).

In this paper, we attempt to provide a plausible reason for the large angle deviation in PLL upon a 30% voltage dip in the nearby transmission system. We demonstrate large angle deviations by using an EMT testbed. Furthermore, analysis has been conducted to examine the role of frequency support, voltage support, as well grid forming (GFM) control in suppressing the large angle deviation. Our contributions are listed as follows.

- A demonstration testbed with suitable assumptions has been constructed to demonstrate large angle deviation.
- Critical grid parameters and operating conditions that can lead to large angle deviation have been identified.
- Furthermore, the effect of frequency support, voltage support, and grid-forming control on angle deviation is clearly demonstrated and explained.
- Lastly, we derived linear block diagram models for both the grid-following (GFL) inverter interconnection system and the GFM inverter interconnection system. Using the models, how each control block may influence angle deviation can be easily identified. The block diagrams offer additional insights into why an additional frequency-power droop in the GFL can help reduce angle deviation.

The rest of the paper is structured to describe the above four contributions. Section II presents the justification for the testbed and two sets of the simulation results to demonstrate the relationship between grid impedance and large angle deviation. Section III presents the analysis results and examines the role of grid parameters and operating conditions on angle deviation. Section IV examines the role of IBR control on angle deviation. Since the analysis in Section III focuses only on the instant of grid voltage dip, a more comprehensive analysis with inverter outer control and frequency support included is presented in Section V. This analysis reveals the mechanism of PLL angle increase upon grid voltage dip and why the additional frequency control mitigates angle deviation. Finally, Section VI concludes this paper.

II. Testbed Construction

In the beginning of this research, PLL's control parameters and control structures were under scrutiny. It is suspected that a large angle deviation may have something to do with PLL's control parameters and control structures. Various types of PLLs, including the simplest synchronous reference frame (SRF)-PLL with a low-pass filter [6], the PLL used in the MATLAB/Simscape library with a sophisticated structure, and the dual-sequence second-order generalized integrator (SOGI)-PLL [7], were tested for a set of three-phase input voltage.

Computer simulations have been conducted to have a PLL's input three-phase voltage subject to a voltage dip. It is found that if the input voltage experiences a balanced dip, the PLL's output angle does not change at all. When there is an unbalanced voltage dip, e.g., phase a voltage experiencing 50% dip, or both phase b and c experiencing 50% dip, the Simscape PLL and SOGI-PLL do show angle deviation. However, the angle deviation from the initial angle is quite small, less than 2 degrees.

Therefore, it is reasoned that the large angle deviation sensed by PLL indeed reflects the angle deviation of the point of common coupling (PCC) bus, since it is well known that the PLL angle tracks the PCC bus angle. In another word, the dq vectors of the PCC bus voltage indeed experience phase shift. We speculate that the transmission system's 30% voltage dip may indeed cause more than 10 degrees of phase angle change in the PLL output angle of a solar PV farm. To this end, we will construct a testbed to have a GFL-IBR interconnect to an infinite bus through a grid impedance as a simplification of the studied IBR power plant grid integration system. This grid impedance reflects grid strength seen by solar PV. Voltage dip will be applied to the infinite bus's voltage to emulate the real-world scenario. The period of voltage dip is limited to 0.05 s to reflect the impact of the fault, which lasted 3 cycles before clearance.

The grid impedance is chosen to be in the range between 0.2 p.u. to 0.35 p.u. The corresponding short circuit ratio (SCR) observed by the solar PV is 5 to 2.86. This is another reasonable assumption. As indicated by [8], a contribution from ERCOT, a wind farm's PCC bus has an SCR of 4 at the normal condition. In addition to the grid impedance, shunt compensation is assumed at the PCC bus. The admittance is assumed to be 0.14 p.u. The assumption of the existence of shunt compensation is necessary since transmission lines have shunt capacitance, while inverters use shunt capacitor filters.

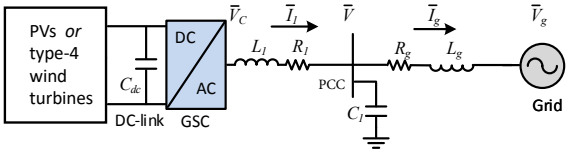


Fig. 1: Circuit topology of a grid-integrated solar PV system.

Fig. 1 shows the circuit topology of the study system. This study system is built in MATLAB/SimScape for EMT simulation. The solar PV farm is represented by a constant dc source interfaced to the ac grid through an inverter. This PV farm is connected to the grid at its PCC bus. The grid is represented as a voltage source behind an impedance R_g+sL_g.

At the PCC bus, a step-up transformer is connected to raise the voltage level from 400 V to 13.2 kV. The inverter is operated by a grid-following controller that regulates the real power and ac voltage magnitude at the PCC bus. The GFL control structure is presented in Fig. 2. A PLL is deployed to synchronize the GFL inverter with the grid by tracking the PCC bus voltage phase angle. Fig. 3 presents the topology of basic three-phase SRF-PLL.

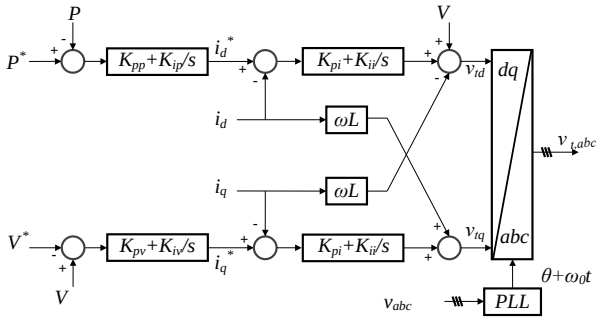


Fig. 2: Grid-following inverter control scheme.

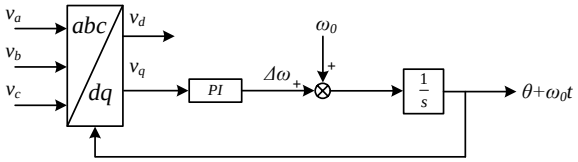


Fig. 3: Block diagram of three-phase SRF-PLL.

The parameters are listed in Table I.

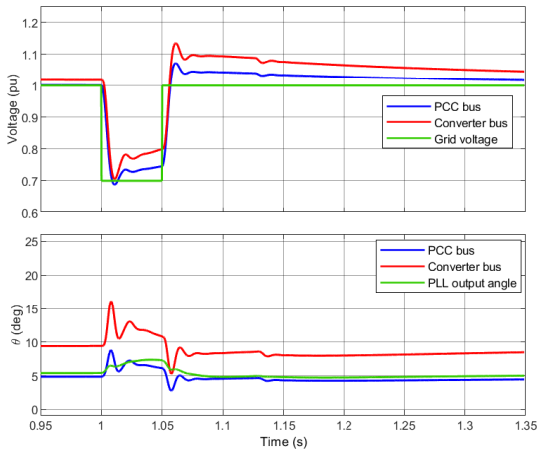
TABLE I: Parameters of the testbed

Description	Value (p.u.)
Choke Resistance, R	0.034
Choke Inductance, L	0.071
Shunt Capacitor, C_1	0.142
Line Resistance, R_g	$X_g/5$
Line Inductance, X_g	0.35
GFL: PLL's PI controller	$60 + 1400/s$
GFL: Real power control	$0.25 + 25/s$
GFL: AC voltage control	$0.4 + 40/s$
GFL/GFM: Current control	$0.4758 + 3.2655/s$
GFM: Angle control	$5 + 20/s$
GFM: AC voltage control	$0.4 + 40/s$

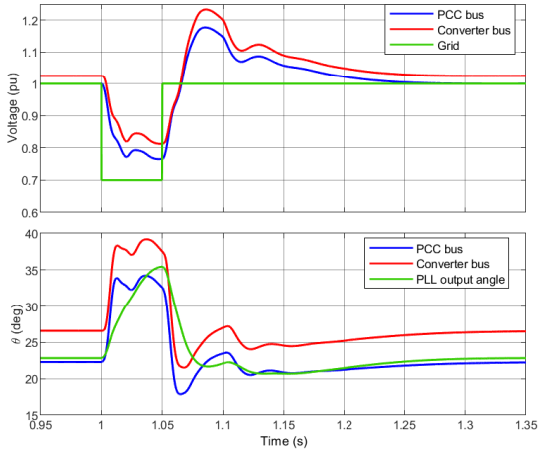
The inverter's outer control regulates real power and ac voltage and generates dq-axis current orders. A 110% current magnitude limit is imposed for the current orders. If the limit is hit, the current orders are scaled down accordingly. The control logic will be further explained along with the simulation results.

Comparison of grid impedance (0.05 pu vs. 0.35 pu) on phase angles upon 30% grid voltage dip is conducted and the simulation results are shown in Figs. 4a and 4b. The figures show the simulation results of the voltages of the three buses (grid, PCC, converter), the angles (the PCC bus and the converter bus), and the PLL output angle. It can be clearly seen that the PCC bus' phase angle jump is less than 5 degrees if the grid impedance is 0.05, while it is more than 10 degrees if the grid impedance is 0.35 pu.

Fig. 5 shows the current orders before and after the current limiting control logic. It can be seen that upon the grid voltage dip, the q-axis current order decreases. This is caused by the PCC voltage reduction and the ac voltage control logic (shown in Fig. 2). At the mean time, the d-axis current order increases due to the real power control logic (also shown in Fig. 2). Between 1.025s and 1.09s, the current magnitude's limit is hit and the dq-axis current orders are scaled down.



(a)



(b)

Fig. 4: Voltage magnitudes and phase angles upon grid voltage dip. (a) $X_g = 0.05$ pu. (b) $X_g = 0.35$ pu.

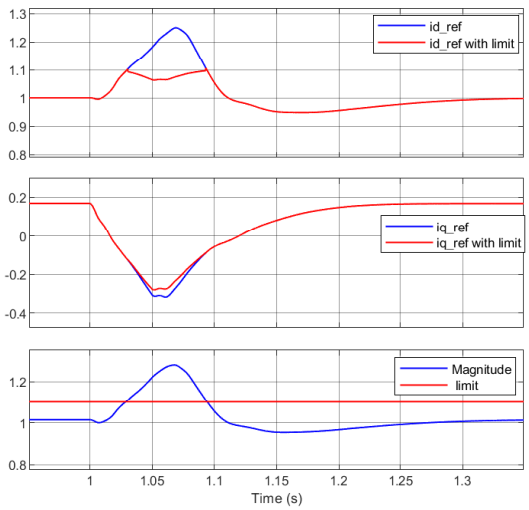


Fig. 5: Current orders before and after the limiting control logic. $X_g = 0.35$ pu.

III. Analysis of Influencing Factors: Grid Strength and Operating Conditions

In this section, we provide analysis focusing on the instant of grid voltage dip. For simplicity, the solar PV is assumed to be connected to a grid represented by a Thévenin equivalent: a constant voltage source behind an impedance jX_g. The solar PV is treated as a current source $i_d + ji_q$ in the PLL frame whose d-axis is aligned with the PCC voltage at steady state. Such treatment has been used in the prior work of weak grid stability analysis [9] and PLL-related transient stability analysis [3]. If the PCC bus voltage phasor and the infinite bus voltage phasor have an angle difference of θ_{PCC}, then the PCC bus voltage phasor is notated as $Ve^{j\theta_{\text{PCC}}}$, while the infinite bus's voltage phasor is notated as $V_g e^{j0}$. Under the normal condition, the following equation exists:

$$\overline{V} = Ve^{j\theta_{\text{PCC}}} = jX_g(i_d + ji_q)e^{j\theta} + V_g, \tag{1}$$

where θ is the PLL's output angle.

At the steady-state condition, the PLL angle exactly tracks the PCC bus voltage angle. Hence $\theta = \theta_{\text{PCC}}$. Separating the real and the imaginary parts, we get

$$V = -X_g i_q + V_g \cos\theta_{\text{PCC}} \tag{2}$$

$$0 = X_g i_d - V_g \sin\theta_{\text{PCC}}. \tag{3}$$

Upon a grid voltage voltage dip, the PLL angle does not jump due to the integrators in its control structure. If i_d and i_q are assumed not changing, then

$$V_g' = V_g - \Delta V_g, \tag{4}$$

$$\overline{V}' = \overline{V} - \Delta V_g, \tag{5}$$

where the superscript $'$ notates symbols after the grid voltage dip.

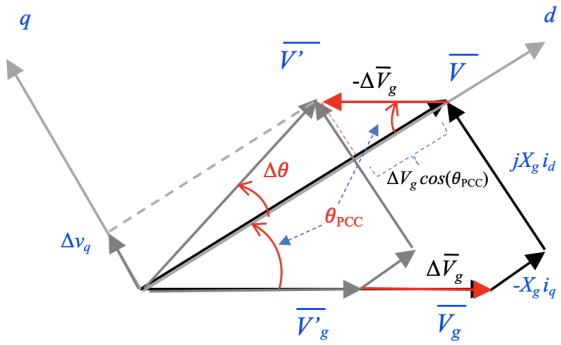


Fig. 6: The PCC voltage vector before and after grid voltage dip in the same dq frame.

Fig. 6 shows the relationship between the dq currents, the grid and PCC bus voltage phasors before and after the grid voltage dip. It can be seen that the PCC bus voltage vector after the dip $\overline{V}'$ is the sum of the $\overline{V}$ and $-\Delta V_g$. Based on Fig. 6, it can be easily seen that

$$\Delta\theta = \tan^{-1}\frac{\Delta V_g \sin\theta_{\text{PCC}}}{V - \Delta V_g \cos\theta_{\text{PCC}}}. \tag{6}$$

Indeed, Fig. 6 implicates that the grid voltage dip results in an immediate phase angle jump for the PCC bus voltage. This has also been confirmed by the simulation results shown in Fig. 4b, where the PCC bus angle has an immediate increase

for more than 10 degrees in less than 10 ms, while the PLL angle rises to the maximum in 50 ms.

If the effects of i_d and i_q are included, and the voltage vectors are viewed from the d-axis in Fig. 6, then the PCC voltage vector after the grid voltage dip can be expressed as:

$$\overline{V}' = jX_g[(i_d + \Delta i_d) + j(i_q + \Delta i_q)] + (V_g - \Delta V_g)e^{-j\theta_{\text{PCC}}} \tag{7}$$

Separating the real and imaginary parts leads to the following:

$$\Delta v_d = -\Delta V_g \cos\theta_{\text{PCC}} - X_g \Delta i_q \tag{8}$$

$$\Delta v_q = \Delta V_g \sin\theta_{\text{PCC}} + X_g \Delta i_d \tag{9}$$

It can be seen that the new PCC voltage vector no longer aligns with the original PCC voltage vector. The angle deviation can be found as

$$\begin{aligned}\Delta\theta &= \tan^{-1}\frac{\Delta v_q}{V - \Delta v_d} \\ &= \tan^{-1}\frac{\Delta V_g \sin\theta_{\text{PCC}} + X_g \Delta i_d}{V - \Delta V_g \cos\theta_{\text{PCC}} - X_g \Delta i_q}\end{aligned} \tag{10}$$

It can be seen that the angle deviation or the change in the q-axis voltage Δv_q has to do with the voltage dip degree, the initial PCC voltage angle θ_{PCC} that is influenced by the grid strength and power exporting level, and the change in dq-axis currents.

Remarks: Based on the above analysis, the critical factor contributing to large angle deviation is indeed $\Delta V_g \sin\theta_{\text{PCC}}$. The following elements influence this critical factor:

1) grid voltage dip degree,
2) grid impedance or grid strength,
3) solar PV's exporting level.

If the grid is very strong, or the grid impedance is very small, the PCC voltage angle θ_{PCC} is also small. If the grid is relatively weak and the solar PV is exporting low power, θ_{PCC} is still small. Hence, even with a 30% voltage dip, the q-axis voltage and in turn the PCC voltage angle will experience insignificant change.

Under the condition of a relatively weak grid and a high exporting power level, a large angle deviation may be possible. In addition, PLL's own parameters should also influence the angle deviation. With the same increase in v_q, large gains of PLL are expected to produce larger angle deviation.

The time-domain simulation results are presented in Fig. 7, showing the grid voltage magnitude v_g, the PCC bus d-axis and q-axis voltages v_d and v_q viewed from the PLL frame (subplot 1); the PLL's output angle in degree (subplot 2), which is relative to the grid voltage; the PLL's output frequency in Hz (subplot 3); the dq-axis currents viewed from the PLL frame (subplot 4); and the real and reactive power from the solar PV (subplot 5).

The grid impedance parameters are $X_g = 0.35$ p.u., and $R_g = 0.2X_g$. In the beginning, solar PV is sending out low power. The PLL's output phase angle is very small, close to 0 degree. At $t = 0.5$ s, the grid voltage reduces from 1 p.u. to 0.70 p.u. This low voltage lasts for 0.05 s and the grid voltage recovers after $t = 0.55$ s. During the voltage dip period, the PLL angle is subject to a few degrees of change since θ is very small.

At $t = 1$ s, the solar PV's power order increases to 1 p.u., and the solar PV is exporting full power. The PLL's angle now becomes 20 degrees. From 1.5 s to 1.55 s, the grid voltage again reduces to 0.70 p.u. After 1.55s, the grid voltage recovers to 1 p.u. It can be seen that the PLL angle reaches a maximum of 33.4 degrees at about 1.55 s.

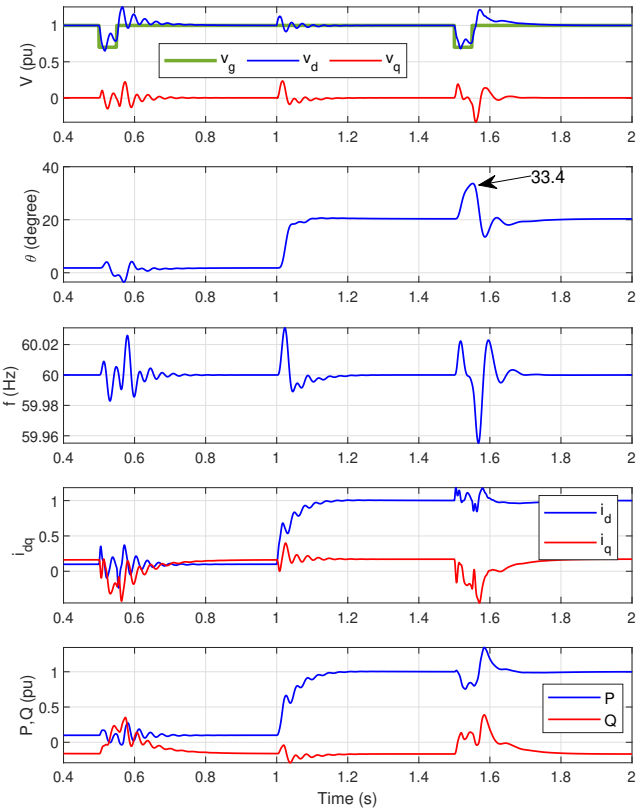


Fig. 7: Simulation results. Events: 30% grid voltage during 0.5 s to 0.55 s; power order increases to 1 p.u. at 1 s; 30% grid voltage during 1.5 s to 1.55 s.

For comparison, the following factors have been examined: PLL parameters and grid strength. Case 1 is the base case with the parameters of Table 1. In Case 2, the PLL's PI controller changes from $60 + 1400/s$ to $20 + 200/s$. In Case 3, the grid impedance reduces from 0.35 p.u. to 0.20 p.u. while the PLL's PI controller is $60 + 1400/s$. Fig. 8 shows the dynamic responses of v_q and θ for the three cases.

It can be seen that larger PLL gains can lead to larger PLL angle deviation in 0.05 seconds. The weaker grid also leads to a larger angle deviation. The simulation results corroborate the remarks based on the analysis.

IV. Influencing Factors: Converter Control

In the previous section, it is revealed that the angle deviation can be large in GFL inverters when experiencing grid voltage dips. In this section, we further examine how converter control may influence angle deviation.

Based on (10), it can be seen that an increase in i_d and an increase in i_q can all lead to angle increase. During a grid

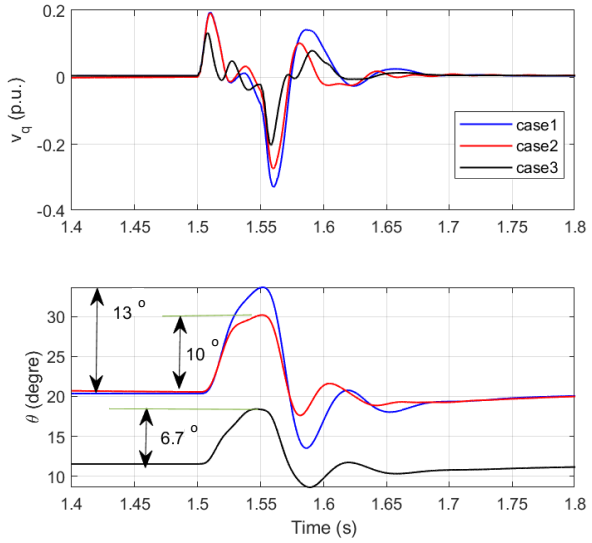


Fig. 8: Effect of PLL parameters and grid strength on v_q and the PLL angle deviation.

voltage dip fault, the real power reduces and the d-axis current order increases due to the d-axis outer control logic. On the other hand, the PCC voltage drops and the ac voltage control leads to a reduced i_q. Therefore, the d-axis outer control may increase the angle deviation while the q-axis outer control may mitigate the angle deviation. It is obvious to see that a slower real power control and a faster ac voltage control lead to less angle deviation. In this section, we examine the control effect on angle deviation and pay particular attention on how controls influence i_d and i_q during faults.

In the following subsections, first, a GFM inverter will be examined for its dynamic performance upon grid voltage dip. Second, GFL with enhanced control will be examined. Finally, voltage control versus reactive power control are compared.

A. GFM

GFM and GFL's key difference is the synchronization scheme. GFL relies on a PLL or voltage-based synchronization, while GFM utilizes power to generate frequency and angle for synchronization. In this subsection, simulation studies are carried out to compare the performances of GFM and GFL under grid voltage dips.

The testbed circuit topology is identical to the GFL testbed. Fig. 9 shows the GFM controller scheme. This control scheme is very similar to a GFL control shown in Fig. 2, except the synchronization unit and the d-axis outer control. The inner current control and the q-axis outer control remain unchanged from the GFL controller. For synchronization, the P-f droop is adopted to generate frequency and angle based on real power measurement. To enforce the angle to be aligned to the PCC bus voltage angle at steady state, the d-axis outer control enforces the q component of the PCC bus voltage v_q to 0. This GFM strategy has been proposed by EPRI in [10] to model GFM in generic IBR models. The GFM control scheme is also very similar to the universal structure presented in [11]. The P-f droop gain is set to be 5% p.u. per p.u. or $5\% \times 377$ rad/s per p.u.

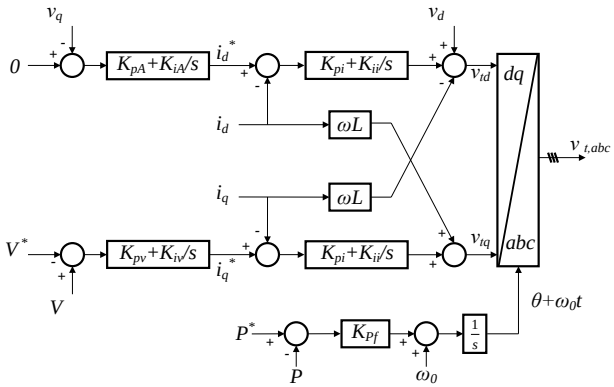


Fig. 9: Grid-forming inverter controller: P-f droop and outer dq voltage control loop.

B. GFL with frequency support control

The above GFM can provide frequency support through P-f droop control, while the GFL is not equipped with frequency support. For a fair comparison, the GFL is also enhanced with frequency support. Frequency support can be introduced by a frequency droop implemented as shown in Fig. 10. The frequency measured by the PLL will be compared with the nominal frequency. If the frequency is below the nominal value, the power order of the d-axis control will be increased. Otherwise, the power order will be decreased.

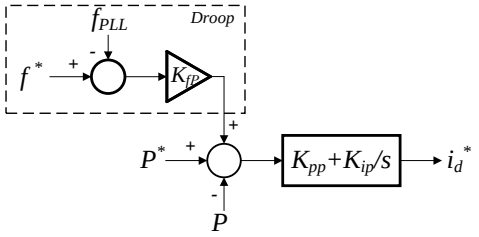


Fig. 10: Block diagram of real power control with frequency support.

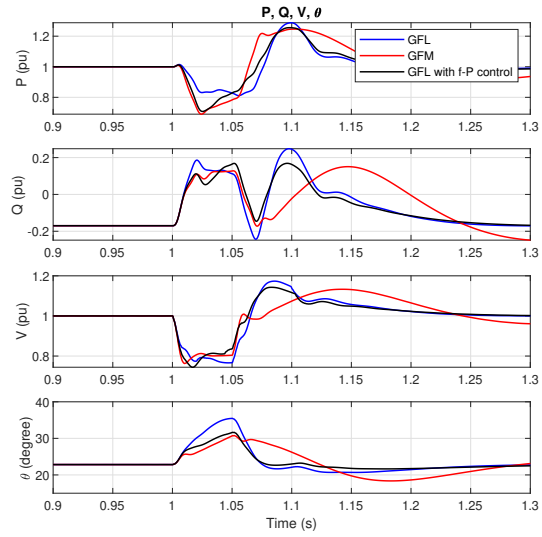
Since the GFM employs P-f droop while the GFL employs f-P droop, the two gains are reciprocal to each other in per unit. If the GFM adopts a gain of 0.05 p.u. , the GFL should adopt a gain of 20 p.u.:

$$K_{\mathrm{fP}} = \frac{1}{K_{\mathrm{Pf}}}. \tag{11}$$

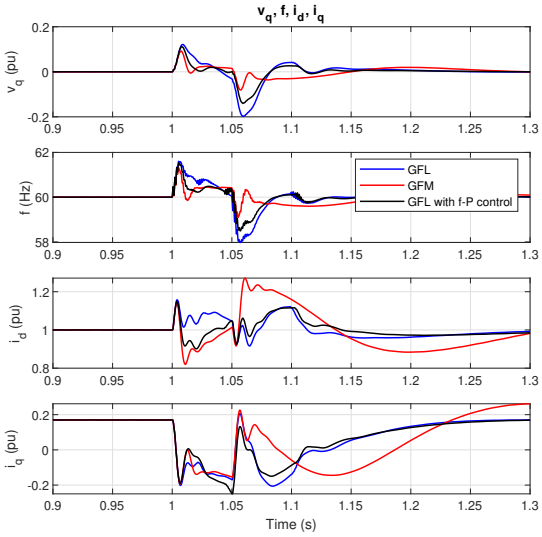
It is worth mentioning that the frequency control is implemented in the inverter level and is considered very fast. A smaller gain leads to insignificant impact. Also in many cases, the frequency control is implemented in the plant-level control and there is communication delay (greater than 0.1 s) to send the power order generated by the frequency control to the inverter level [12]. The effect of delay makes the frequency control much slower.

For comparison, three simulation testbeds with the same grid strength and same generator operating conditions are examined for the same grid voltage dip. The output power is 1 pu, the PCC bus voltage is regulated at 1 pu, and the grid impedance X_g is 0.35 pu.

Fig. 11 presents the dynamic responses of GFL with or without frequency droop control and GFM during the same



(a)



(b)

Fig. 11: Comparison of GFL, GFM, and GFL with frequency support control: (a) P, Q, V, and θ. (b) v_q, f, i_d, and i_q.

grid voltage dip event. Grid voltage dips to 70% at 1 second and gets cleared after 0.05 seconds. All the measurements are generated by an SRF-PLL with the same specifications.

Fig. 11a shows the real power, reactive power, PCC voltage magnitude, and angle measurements. Fig. 11b shows the q-axis voltage, frequency, and dq current components. Based on the comparisons presented in Fig. 11, the angle deviation of GFM is found to be 5 degrees smaller than that of the GFL inverter. When the frequency droop control is enabled in the GFL, it is found that the frequency droop control can achieve the same effect of angle deviation reduction.

While all three converters show similar voltage responses during the fault period, their responses in i_d show significant differences. Due to voltage drop and real power reduction upon fault, the GFL's d-axis outer control sees a positive error and tries to bring i_d up. On the other hand, with frequency support control enabled, upon the fault condition, the power reference will not keep the same. Rather the power reference to the d-axis outer control will decrease since the measured frequency has an immediate increase. Therefore, the inverters with frequency support are shown to have lower power and lower i_d during the fault period compared to the GFL. According to the analysis equation (10), a smaller Δi_d mitigates angle deviation.

Two important remarks are drawn.

1) Frequency support control can reduce angle deviation.
2) How an inverter is synchronized to the grid, whether it is voltage-based or power-based, has an insignificant influence on angle deviation.

C. Voltage Support

In addition to the frequency support, we also examine the influence of voltage support. Besides real power and voltage vector control, real and reactive power vector control is also very common in GFL inverters. Without changing the control parameters, the existing voltage control is replaced by reactive power control. A side-by-side comparison is then performed at 1 p.u. of output power and 1 p.u. of PCC voltage magnitude. The comparison is shown in Fig. 12.

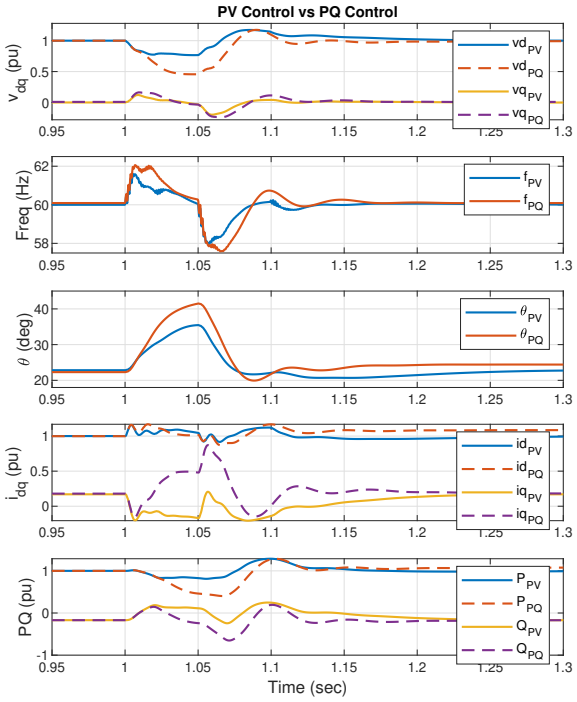


Fig. 12: Different GFL control strategies are compared: PV control vs PQ control.

After replacing the voltage control with reactive power control, the voltage support is even weaker, which leads to larger deviations in all monitored components. it can be seen that the change in the q-axis outer control leads to significant change and in turn different reactive power support. With voltage control, more reactive power support is provided. Hence, a higher PCC voltage is maintained during fault. It can be seen that less voltage support is harmful when GFL

experiences voltage dips. This observation corroborates (10) that an increase in i_q (corresponding to less reactive power support) leads to larger angle deviation.

Therefore, stronger voltage support is examined next. The voltage control of $1 + 100/s$ is applied to the GFL controller. Re-run the simulation, and the results are compared in Fig. 13. Faster voltage control indicates stronger voltage support. And based on the comparison, it shows that the extra voltage support can mitigate the maximum angle deviation by about 3 degrees.

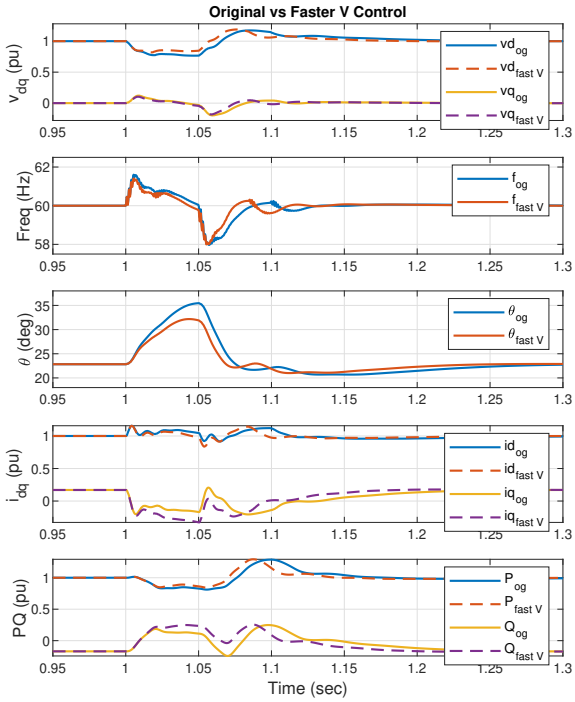


Fig. 13: Different voltage control gains in use: original vs faster voltage control.

Remarks: The comparison case studies show that voltage support helps mitigate angle deviation.

This finding aligns with the finding on fast voltage control's benefit in improving small-signal stability for IBRs in weak grids [13].

V. Further Analysis

The analysis shown in Section III focuses on the instant of grid voltage dip. The effect of outer controls and frequency-power droop control have not been included. A comprehensive analysis is presented in this section. The goal is to develop quantitative analysis of the effect of grid voltage dip on angle deviation and the effect of frequency-power droop control in both GFL and GFM.

To start, we derive the block diagrams for two types of inverters with different synchronization methods: voltage-based and power-based. With derived block diagrams, the linear model describing the angle vs. the grid voltage can be found. The derived models will be compared with the ones identified from the data generated by the EMT testbed. Based on the two sets of the models, same conclusions on the influence of parameters are expected to be drawn.

A. Block Diagram Derivation

The block diagram is based on the assumption that the converters can be treated as current sources. This assumption is justified as both GFL and GFM have employed current control and the current control bandwidth is much higher compared to other controls. This simplification is necessary for symbolic derivation and has been adopted in block diagram derivation for stability analysis of wind farms in a weak grid by the first author [14] and for control interaction analysis involving PLL in [15]. An overly complicated block diagram loses its meaning to develop insights. On the other hand, the frequency responses obtained from the block diagrams will be compared to those obtained from the EMT testbeds for verification.

For both inverters, controls are in a dq-frame different from the grid dq-frame which has a constant speed. The control frame does not have a constant rotating speed during transients. In the grid frame, the voltage and current relationship is expressed as follows.

$$\overline{V} = Ve^{j\theta_{\rm PCC}} = \overline{V}_g + jX_g(i_d + ji_q)e^{j\theta} \tag{12}$$

where $\theta_{\rm PCC}$ is the PCC bus voltage angle while θ is the output angle of the synchronization unit. In GFL, this angle is the PLL's output angle; while in GFM, this angle is generated through P-f droop control followed by an integrator. The PCC bus angle and the inverter's angle are the same at the steady state but different during transients.

The above equation is now expressed in the control dq frame.

$$\begin{aligned} Ve^{j(\theta_{\rm PCC}-\theta)} &= V_g e^{-j\theta} + jX_g(i_d + ji_q) \\ v_d &= V\cos(\theta_{\rm PCC} - \theta) = V_g\cos\theta - X_g i_q \\ v_q &= V\sin(\theta_{\rm PCC} - \theta) = -V_g\sin\theta + X_g i_d \end{aligned} \tag{13}$$

Note that at steady state, $\theta_{\rm PCC} = \theta$. Hence,

$$\begin{aligned} v_d &= V = V_g\cos\theta - X_g i_q \\ v_q &= 0 = -V_g\sin\theta + X_g i_d \end{aligned} \tag{14}$$

The linear relationship of the control frame voltages (v_d and v_q), voltage magnitude V and angle $\theta_{\rm PCC}$, the control frame currents (i_d and i_q), and the output angle θ can be found as follows.

$$\begin{aligned} \Delta v_d &= \Delta V = \cos\theta\Delta V_g - V_g\sin\theta\Delta\theta - X_g\Delta i_q \\ \Delta v_q &= V(\Delta\theta_{\rm PCC} - \Delta\theta) \\ &= -\sin\theta\Delta V_g - V_g\cos\theta\Delta\theta + X_g\Delta i_d \end{aligned} \tag{15}$$

The block diagrams can be developed with the real power expression ($\Delta P = V\Delta i_d + i_d\Delta v_d$), the outer controls, and the synchronization unit added. Fig. 14a shows the GFL system's block diagram while Fig. 14b shows the GFM system's block diagram. The two systems share many similarities except for the two blocks: the synchronization unit and the d-axis control input. In the GFL, the angle θ is generated by the PLL, more specifically, by passing v_q to a PI controller followed by an

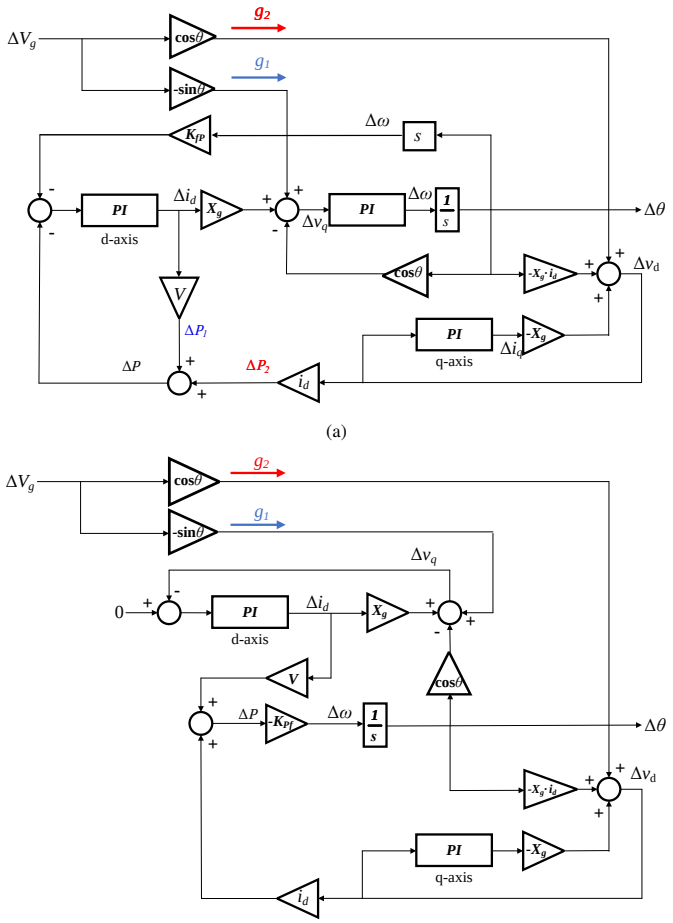


Fig. 14: Block diagrams. (a) GFL. (b) GFM.

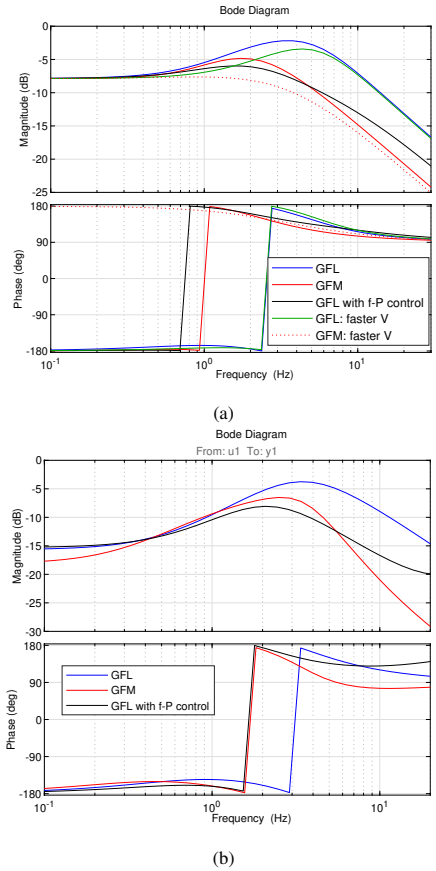


Fig. 15: Bode diagrams $\Delta\theta/\Delta V_g$. (a) Block diagram based. (b) EMT measurement based.

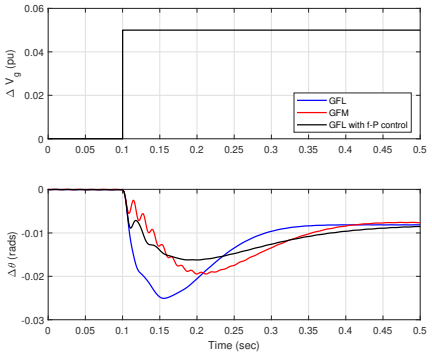


Fig. 16: Measurement data collected from the EMT testbeds.

integrator. In the GFM, the angle θ is generated by the power-frequency droop control followed by an integrator. The d-axis control input is the real power and v_q, in the GFL and GFM, respectively.

B. Comparison with the models identified from data

With the input as the grid voltage ΔV_g while the output as the angle $\Delta\theta$, the input/output transfer function can be obtained by use of the block diagram. Five cases are examined:

- case 1 GFL: GFL without P-f droop control and with the base case parameters.
- case 2 GFM: GFM with f-P droop (2%) and base case parameters.
- case 3 GFL with P-f droop: GFL with P-f droop control (50) and with the base case parameters.
- case 4 GFL: faster V: GFL without P-f droop control. Its voltage control is changed to be $1 + 100/s$.
- case 5 GFM: faster V: GFM with f-P droop (2%) and its voltage control is changed to be $1 + 100/s$.

The Bode diagrams are presented in Fig. 15(a).

For comparison, measurements are collected from the EMT testbeds. V_g is perturbed by 5% of step increase and the angle θ's responses are collected for the first three cases. The measurement data are presented in Fig. 16. Based on the three sets of input/output data, the linear models are estimated using MATLAB System Identification Toolbox's `tfest` function. This function uses a refined least square estimation method — instrumental variables method [16]–to conduct model estimation through data fitting.

The resulting models' Bode diagrams are shown in Fig. 15(b). Due to the omission of resistance of the transmission line, the magnitudes of the derived transfer functions at steady state are all higher compared to those of the EMT models. On the other hand, compared to the linear models extracted from the EMT testbed, the derived linear models (which has ignored transmission line resistance, transmission line dynamics, and

current controls) can successfully capture the influence of frequency control in the 0.1-Hz to 20-Hz region.

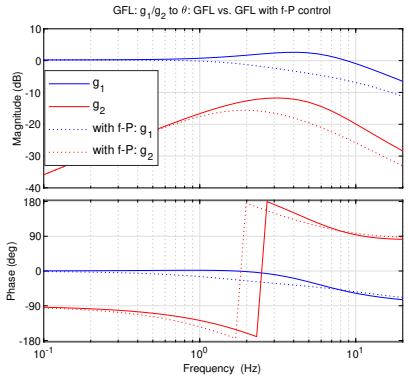
Remarks:

1) Bode diagrams based on both the derived model and the model identified from computer simmulation data show that frequency control reduces the bandwidth and magnitudes. This makes the angle change slower with less amplification when frequency control is enabled, whether this is implemented in the GFL or GFM.
2) Based on the Bode diagrams in Fig. 15(a), it can be seen that faster voltage control reduces the peak magnitude while not changing the bandwidth of the system. Therefore, fast voltage control can show reduced angle deviation.

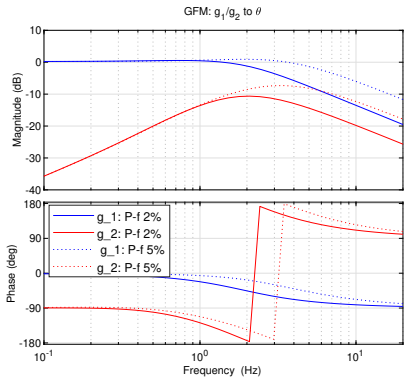
C. Effect of frequency-power droop control

For GFL, it can be seen from both the analysis results in Fig. 15 and EMT simulation results in Fig. 11 and Fig. 13 that frequency control appears to reduce angle deviation more effectively compared to faster voltage control. Further analysis is provided to offer an explanation on why frequency control helps reduce angle deviation.

Fig. 17a shows the contributions to $\Delta\theta$ from g_1 and g_2 (where $g_1 = -\sin\theta\Delta V_g$ and $g_2 = \cos\theta\Delta V_g$) for the GFL system. Fig. 17b shows the contributions to $\Delta\theta$ from g_1 and g_2 in the GFM system.



(a)



(b)

Fig. 17: Contributions to angle deviation by g_1 and g_2. (a) GFL. (b) GFM.

It can be clearly seen from Fig. 17a that in GFL, the contribution from g_1 is dominant. When f-P control is enabled, the magnitude of g_1 to $\Delta\theta$ reduces more than 3 dB in the 3 Hz above region. This implies that the angle change is dominantly influenced by the influence of grid voltage dip in v_q (g_1) in the GFL case. The influence of grid voltage dip on v_d (g_2) follows the path to first decrease real power and then increase i_d through the d-axis control.

When there is no f-P control, and the influence from g_2 and v_d is ignored, g_1's influence can be found as

$$\frac{\Delta\theta}{g_1} = \frac{\left(K_{p,\mathrm{PLL}} + \frac{K_{i,\mathrm{PLL}}}{s}\right)\frac{1}{s}}{1 + \cos\theta\left(K_{p,\mathrm{PLL}} + \frac{K_{i,,\mathrm{PLL}}}{s}\right)\frac{1}{s}} \approx G_{\mathrm{PLL}}(s). \quad (16)$$

The above transfer function equals the closed-loop PLL's transfer function if $i_q = 0$. Therefore, if PLL's response is very fast, the angle deviation will be more severe. Also, the angle deviation depends on g_1. g_1 is greater if θ (the angle between the PCC bus voltage and the grid) is larger.

When the f-P droop control is enabled, negative feedback is added from θ to g_1. With the effect from g_2 (in turn ΔP_2) ignored, the closed-loop transfer function from g_1 to θ becomes the following:

$$\frac{\Delta\theta}{g_1} = \frac{G_{\mathrm{PLL}}}{1 + G_{\mathrm{PLL}} \times s \times \frac{K_{\mathrm{fP}}}{377}\frac{1}{1+0.05s}X_g} \quad (17)$$

Note that the low-pass filter $\frac{1}{1+0.05s}$ is used to approximate the transfer function from the inverter power command ΔP^* to Δi_d with the effect of PCC voltage influence on power ignored ($\Delta P_2 \approx 0$):

$$\frac{\Delta i_d}{\Delta P^*} = \frac{K_{pP} + \frac{K_{iP}}{s}}{1 + V\left(K_{pP} + \frac{K_{iP}}{s}\right)} \approx \frac{1}{1 + 0.05s}, \quad (18)$$

when the real power PI control is $0.25 + 25/s$.

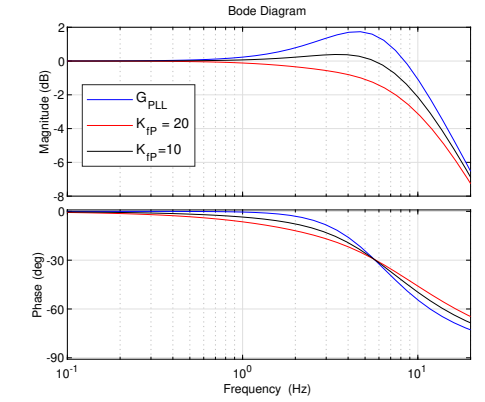
Fig. 18a shows the Bode diagrams of G_{PLL} and $\frac{\Delta\theta}{g_1}$ for different K_{fP} parameters when $X_g = 0.35$ p.u. It can be seen that The f-P droop essentially works as a feedback loop to reduce the bandwidth and the magnitude of $\Delta\theta/g_1$. The larger the f-P droop gain, the more reduction in the magnitude and bandwidth, implying slower angle response and less angle deviation upon grid voltage dip. Fig. 18b further shows the EMT testbed simulation results of PLL angle upon 30% grid voltage dip. It can be seen that the larger the f-P gain, the more reduction in angle deviation.

In the GFM, it can be seen from Fig. 17b that g_1's influence on θ is also greater than g_2's. Further, a smaller P-f droop gain or stronger frequency support is shown to lead to smaller magnitudes in the above 1 Hz region, implying less angle deviation upon grid voltage dip.

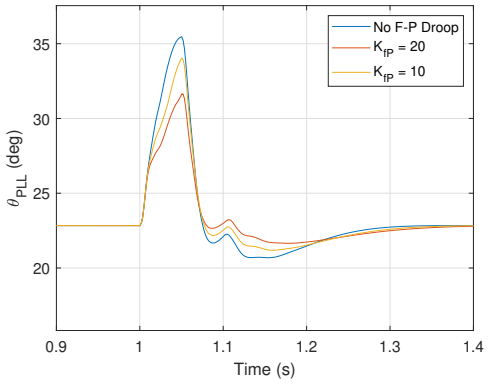
Remarks: Based on the frequency-domain responses from the grid voltage to the inverter angle, it can be seen that frequency support reduces the magnitude and bandwidth while voltage support reduces the magnitude. Both measures help mitigate large angle deviation upon grid voltage dip.

VI. Conclusion

In this paper, we investigated the influencing factors of large inverter angle deviation observed in real-world solar PV tripping events. Our investigation shows that large angle



(a)



(b)

Fig. 18: (a) Comparison of $\frac{\Delta\theta}{g_1}$ with and without f-P control. (b) EMT simulation results of PLL angle upon 30% grid voltage dip.

deviation may occur in grid-following inverters upon grid voltage dip under several conditions: a relatively large grid impedance, high exporting power level, and large PLL gains. In addition, it is found that frequency support control, regardless of synchronizing methods can reduce angle deviation in the fault duration period. Faster voltage control also helps mitigate large angle deviation.

REFERENCES

[1] Joint NERC and Texas RE Staff Report. (2021, September) Odessa Disturbance.

[2] Ö. Göksu, R. Teodorescu, C. L. Bak, F. Iov, and P. C. Kjær, "Instability of wind turbine converters during current injection to low voltage grid faults and PLL frequency based stability solution," *IEEE Transactions on Power Systems*, vol. 29, no. 4, pp. 1683–1691, 2014.

[3] X. He, H. Geng, R. Li, and B. C. Pal, "Transient stability analysis and enhancement of renewable energy conversion system during LVRT," *IEEE Transactions on Sustainable Energy*, vol. 11, no. 3, pp. 1612–1623, 2019.

[4] H. Geng, L. Liu, and R. Li, "Synchronization and reactive current support of PMSG-based wind farm during severe grid fault," *IEEE Transactions on Sustainable Energy*, vol. 9, no. 4, pp. 1596–1604, 2018.

[5] J. Chen, M. Liu, H. Geng, T. O'Donnell, and F. Milano, "Impact of PLL frequency limiter on synchronization stability of grid feeding converter," *IEEE Transactions on Power Systems*, vol. 37, no. 3, pp. 2487–2490, 2022.

[6] L. Fan, Z. Miao, and Z. Wang, "A new type of weak grid IBR oscillations," *IEEE Transactions on Power Systems*, vol. 38, no. 1, pp. 988–991, 2022.

[7] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "A new single-phase PLL structure based on second order generalized integrator," in *2006 37th IEEE Power Electronics Specialists Conference*, 2006, pp. 1–6.

[8] S.-H. Huang, J. Schmall, J. Conto, J. Adams, Y. Zhang, and C. Carter, "Voltage control challenges on weak grids with high penetration of wind generation: Ercot experience," in *2012 IEEE Power and Energy Society General Meeting*. IEEE, 2012, pp. 1–7.

[9] L. Fan and Z. Miao, "An explanation of oscillations due to wind power plants weak grid interconnection," *IEEE trans. Sustainable Energy*, vol. 9, no. 1, pp. 488–490, 2018.

[10] D. Ramasubramanian, E. Farantatos, O. Ajala, S. Dhople, and B. Johnson, "A universal grid-forming inverter model and simulation-based characterization across timescales," in *Hawaii International Conference on System Sciences 2023*, 2023.

[11] L. Harnefors, J. Kukkola, M. Routimo, M. Hinkkanen, and X. Wang, "A universal controller for grid-connected voltage-source converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 5, pp. 5761–5770, 2021.

[12] L. Fan, Z. Miao, D. Ramasubramanian, and H. Ding, "Operational challenges of solar pv plus storage power plants and modeling recommendations," *IEEE Open Access Journal of Power and Energy*, pp. 1–1, 2023.

[13] Y. Li, L. Fan, and Z. Miao, "Stability control for wind in weak grids," *IEEE Trans. Sustainable Energy*, vol. 10, no. 4, pp. 2094–2103, 2019.

[14] L. Fan, "Modeling type-4 wind in weak grids," *IEEE trans. Sustainable Energy*, vol. 10, no. 2, pp. 853–864, 2019.

[15] Y. Huang, X. Yuan, J. Hu, and P. Zhou, "Modeling of vsc connected to weak grid for stability analysis of dc-link voltage control," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, no. 4, pp. 1193–1204, 2015.

[16] A. A. Ozdemir and S. Gumussoy, "Transfer function estimation in system identification toolbox via vector fitting," *IFAC-PapersOnLine*, vol. 50, no. 1, pp. 6232–6237, 2017.

Lingling Fan (Fellow, IEEE) received the B.S. and M.S. degrees in electrical engineering from Southeast University, Nanjing, China, in 1994 and 1997, respectively, and the Ph.D. degree in electrical engineering from West Virginia University, Morgantown, in 2001.

Currently, she is a full professor at the University of South Florida, Tampa, where she has been since 2009. She was a Senior Engineer in the Transmission Asset Management Department, Midwest ISO, St. Paul, MN, form 2001 to 2007, and an assistant professor with North Dakota State University, Fargo, from 2007 to 2009. Her research interests include control, dynamic modeling, and system identification in power systems and power electronics. Dr. Fan serves as the editor-in-chief for IEEE Electrification Magazine and associate editor for IEEE Trans. Energy Conversion.

Zhengyu Wang (Member, IEEE) received the B.S. degree in electrical engineering from Iowa State University, Ames, IA, USA, in 2017. He received the M.S.E.E. degree and the Ph.D. degree from the University of South Florida (Tampa, FL) in 2019 and 2022, respectively. His research interests include inverter-based resource electromagnetic transient-based modeling, simulation, and hardware-in-the-loop experiments. Currently, he is a transmission engineer with RWE Clean Energy at Austin, Texas.

Zhixin Miao (Senior Member, IEEE) received the B.S.E.E. degree from the Huazhong University of Science and Technology,Wuhan, China, in 1992, the M.S.E.E. degree from the Graduate School, Nanjing Automation Research Institute (Nanjing, China) in 1997, and the Ph.D. degree in electrical engineering from West Virginia University, Morgantown, in 2002.

Currently, he is with the University of South Florida (USF), Tampa. Prior to joining USF in 2009, he was with the Transmission Asset Management Department with Midwest ISO, St. Paul, MN, from 2002 to 2009. His research interests include power system protection, real-time digital simulation, and microgrids. Dr. Miao serves as Associate Editor for IEEE trans. Sustainable Energy.