Thévenin Equivalent Representation of Meshed Grids for IBR Dynamic Phenomena Replication

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***Abstract*—Single inverter-based resource (IBR) infinite-bus representation has been adopted for real-world event analysis and replication by the senior authors. In particular, for the 2021 Texas Odessa event, adopting a Thévenin equivalent representation for the main grid and subjecting the grid voltage to a voltage dip enable successful demonstration of IBR bus phase jump. In this article, we provide the justification of the Thévenin equivalent representation by examining a meshed network with and without faults. Using the bus impedance matrix, we present the theoretic analysis that leads to the findings of Thévenin equivalent impedance and voltage before and during the fault. It can be seen that a fault causes dip in the Thévenin equivalent voltage and change in the equivalent impedance. Additionally, we have set up two test circuits, one meshed network with an IBR and another a single-IBR infinite-bus system. We conduct open-circuit and short-circuit tests for the meshed network at the IBR's point of interconnection bus to demonstrate that the Thévenin equivalent representation based on the theoretic analysis matches with the one found from the experiments. Further, we show that for the same IBR, its dynamic performance in a meshed network for a fault is the same as that based on the single-IBR infinite-bus system subject to a voltage dip event.**

***Index Terms*—Inverter-based resources, phase-locked-loop, stability, equivalent modeling.**

I. Introduction

Unexpected large-scale IBR tripping events have occurred upon transmission line faults and reported by North American Electric Reliability Corporation (NERC) [1]–[3]. Additional, many subsynchronous oscillation events events in IBRs have been reported [4]–[6]. In several mechanism analysis investigations conducted by the senior authors [5]–[8], a single-inverter infinite-bus representation has been adopted. Such representation has the analogy of the traditional single-machine infinite-bus (SMIB) representation widely adopted for synchronous generator transient and dynamic analysis.

In particular, for the 2021 Texas Odessa event, adopting a Thévenin equivalent representation for the main grid and subjecting the grid voltage to a voltage dip enables successful demonstration of large PLL angle deviation [9]. In the current paper, we provide the justification of the Thévenin equivalent representation by examining a meshed network with and without faults. Using the bus impedance matrix of a network without the IBR under study, we find the Thévenin equivalent viewed from the IBR point of interconnection (POI) bus at the pre-fault and fault conditions. It can be seen that fault is equivalent to the Thévenin voltage subject to a dip in addition to the Thévenin impedance change. We verify this finding by Thévenin equivalent identified through open-circuit and short-circuit tests. The single-IBR infinite-bus system is built to represent the IBR interconnected to a meshed network. Its dynamic responses in both circuits are compared.

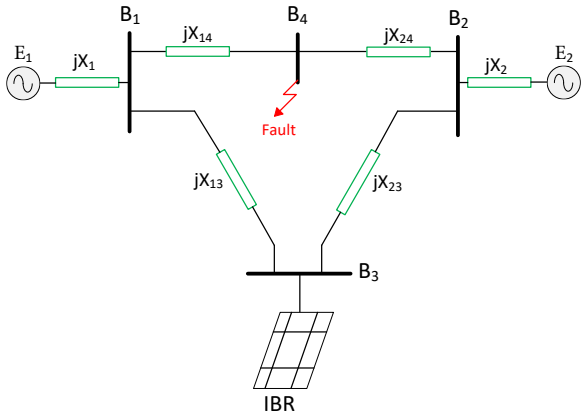
The paper is organized as follows. Section II provides a tutorial example on finding the Thévenin equivalent representation through bus impedance matrix. Section III presents the case study of a meshed network with an IBR. The network is analyzed by use of its bus impedance matrix to calibrate the Thévenin equivalent viewed from the IBR POI bus. Open-circuit and short-circuit experiments are conducted for the network without the IBR. This step is to find the Thévenin equivalent using experiment data and verify the analysis results. Section IV further demonstrates and compares IBR dynamic performance in the single-IBR infinite-bus setup and in the meshed network for a three-phase fault and a single-line-to-ground (SLG) fault. Section V concludes this paper.

II. A tutorial example

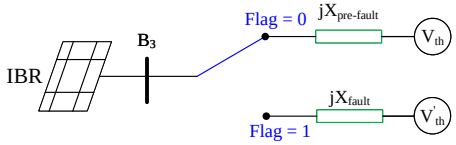
Fig. 1(a) shows an example meshed network. Two synchronous generators are connected to Bus 1 and Bus 2. An IBR is connected at Bus 3. Based on the IBR's point of view, the grid behind Bus 3 can be represented as a Thévenin equivalent circuit. The pre-fault condition and the during-fault condition lead to distinct circuits. We assume a fault will be applied at Bus 4.

Assume that $X_1 = X_2 = X_{13} = X_{23} = 0.2$ and $X_{14} = X_{24} = 0.1$. Also assume that the two voltage sources are of 1 pu at phase angle 0. It can be seen that the bus admittance matrix at the prefault condition is as follows.

$$Y^{\text{pre}} = \begin{bmatrix} -j20 & 0 & j5 & j10 \\ 0 & -j20 & j5 & j10 \\ j5 & j5 & -j10 & 0 \\ j10 & j10 & 0 & -j20 \end{bmatrix} \tag{1}$$



(a)



(b)

Fig. 1: (a) The meshed network. (b) The single-IBR infinite-bus system.

Inverting this matrix leads to the bus impedance matrix.

$$\begin{bmatrix} \overline{V}_1 \\ \overline{V}_2 \\ \overline{V}_3 \\ \overline{V}_4 \end{bmatrix} = j \underbrace{\begin{bmatrix} 0.125 & 0.075 & 0.1 & 0.1 \\ 0.075 & 0.125 & 0.1 & 0.1 \\ 0.1 & 0.1 & 0.2 & 0.1 \\ 0.1 & 0.1 & 0.1 & 0.15 \end{bmatrix}}_{Z_{pre}} \begin{bmatrix} \frac{1}{j0.2} \\ \frac{1}{j0.2} \\ \overline{I}_3 \\ 0 \end{bmatrix} \tag{2}$$

It can be see that

$$\overline{V}_3 = j0.2\overline{I}_3 + 1. \tag{3}$$

Therefore, the Thévenin equivalent impedance is $j0.2$ pu while the voltage source is 1 pu.

When Bus 4 is subject to a 3-phase fault and the fault impedance is assumed to be $j0.1$, the admittance matrix changes to:

$$Y^{\text{fault}} = \begin{bmatrix} -j20 & 0 & j5 & j10 \\ 0 & -j20 & j5 & j10 \\ j5 & j5 & -j10 & 0 \\ j10 & j10 & 0 & -j30 \end{bmatrix} \tag{4}$$

In turn, the Thévenin equivalent impedance changes to $j0.16$ pu while the voltage source changes to 60%.

Therefore, it can be seen the fault condition can be well represented by a Thévenin equivalent circuit and have the voltage source subject to a few cycles of voltage dip, depending on the fault duration. This is the testbed condition set up in [9].

III. A Test Case of Meshed Network

We now examine a 230-kV meshed network test case. This topology of the test case is same as the one in Fig. 1(a). On the other hand, the transmission line are not lossless.

TABLE I: Main Parameters of the System

Description	Item	Value	Per unit
Bus-1 source	E_1	230 kV	1
Bus-1 Angle	θ_1	10°	-
Bus-2 source	E_2	230 kV	1
Bus-2 Angle	θ_2	0°	-
Nominal Frequency	f	60 Hz	-
Line Impedance	$[R\ X]$	-	[0.06 0.2]
IBR DC Voltage	V_{dc}	1000 V	-
IBR Filter Parameter	$[R_f\ L_f]$	[0.001 Ω 46 μH]	[0.0063 0.1084]
GFL d-axis	$[K_{pP}\ K_{iP}]$	-	[0.1 30]
GFL q-axis	$[K_{pQ}\ K_{iQ}]$	-	[0.4 40]
Current Control dq-axis	$[K_{pI}\ K_{iI}]$	-	[0.3 20]
PLL	$[K_p\ K_i]$	-	[60 1400]

The test case has two conventional generators connected to Bus 1 and Bus 2, and an IBR connected at Bus 3. The two generators are represented by constant voltage sources. The $\frac{R}{X}$ ratio of all impedance is assumed to be 0.3. Any transient caused by the fault would be damped out in 6 cycles.

Additionally, the IBR is connected to the POI bus through a transformer. Fig. 2 shows the topology of the inverter that is connected to the grid. The inverter output voltage is stepped up to 230 kV to match the voltage of the 4-bus system, as shown in Fig. 1(a). The same IBR will be tested in the single-IBR infinite-bus system, as seen in Fig. 1(b). The IBR is a grid-following IBR equipped with current vector control and synchronized to the grid through phase-locked-loop (PLL). Its outer control regulated real power and reactive power. The detail parameters are presented in Table I.

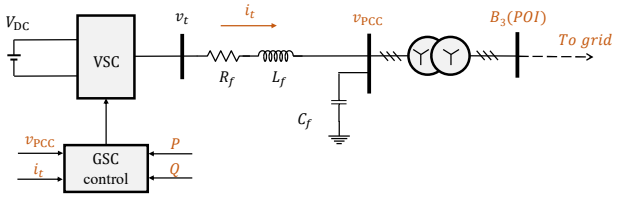


Fig. 2: The inverter topology that is connected to the grid.

A. Bus matrix impedance

The first step in deriving the Thévenin equivalent of a complex system is to construct the admittance matrix (Y-bus). The size of the matrix is determined by the number of buses in the system, and in the modified system, the maximum number of buses is 4, so the generated admittance matrix is 4×4. Since we are interested to find out the Thévenin equivalent of the grid viewed from Bus 3, in the step of admittance matrix construction, the IBR is treated as a current source injection $\overline{I}_3$.

Based on this assumption, the admittance matrix is built (shown in Eq. (5)) with the diagonal elements of the admittance matrix being the sum of all the admittances connected to the corresponding bus, and the non-diagonal elements being the negative admittances connected between the two corresponding buses. The highlighted part is the Bus 4's fault impedance contribution ($Z_{\text{fault}} = j0.1$ pu).

$$\begin{bmatrix} \frac{1\angle 10^\circ}{Z_1} \\ \frac{1\angle 0^\circ}{Z_2} \\ \overline{I}_3 \\ 0 \end{bmatrix} = \begin{bmatrix} \frac{1}{Z_1}+\frac{1}{Z_{14}}+\frac{1}{Z_{13}} & 0 & \frac{-1}{Z_{13}} & \frac{-1}{Z_{14}} \\ 0 & \frac{1}{Z_2}+\frac{1}{Z_{24}}+\frac{1}{Z_{23}} & \frac{-1}{Z_{23}} & \frac{-1}{Z_{24}} \\ \frac{-1}{Z_{13}} & \frac{-1}{Z_{23}} & \frac{1}{Z_{13}}+\frac{1}{Z_{23}} & 0 \\ \frac{-1}{Z_{14}} & \frac{-1}{Z_{24}} & 0 & \frac{1}{Z_{14}}+\frac{1}{Z_{24}}+\frac{1}{Z_{\text{fault}}} \end{bmatrix} \begin{bmatrix} \overline{V}_1 \\ \overline{V}_2 \\ \overline{V}_3 \\ \overline{V}_4 \end{bmatrix} \tag{5}$$

$$\begin{bmatrix} \overline{V}_1 \\ \overline{V}_2 \\ \overline{V}_3 \\ \overline{V}_4 \end{bmatrix} = \underbrace{\begin{bmatrix} 0.0375+0.1250j & 0.0225+0.0750j & 0.0300+0.1000j & 0.0300+0.1000j \\ 0.0225+0.0750j & 0.0375+0.1250j & 0.0300+0.1000j & 0.0300+0.1000j \\ 0.0300+0.1000j & 0.0300+0.1000j & 0.0600+0.2000j & 0.0300+0.1000j \\ 0.0300+0.1000j & 0.0300+0.1000j & 0.0300+0.1000j & 0.0450+0.1500j \end{bmatrix}}_{Z_{\text{pre}}} \begin{bmatrix} \frac{1\angle 10^\circ}{0.06+j0.2} \\ \frac{1}{0.06+j0.2} \\ \overline{I}_3 \\ 0 \end{bmatrix} \tag{6}$$

$$\begin{bmatrix} \overline{V}_1 \\ \overline{V}_2 \\ \overline{V}_3 \\ \overline{V}_4 \end{bmatrix} = \underbrace{\begin{bmatrix} 0.0206+0.0856j & 0.0056+0.0356j & 0.0131+0.0606j & 0.0046+0.0408j \\ 0.0056+0.0356j & 0.0206+0.0856j & 0.0131+0.0606j & 0.0046+0.0408j \\ 0.0131+0.0606j & 0.0131+0.0606j & 0.0431+0.1606j & 0.0046+0.0408j \\ 0.0046+0.0408j & 0.0046+0.0408j & 0.0046+0.0408j & 0.0070+0.0613j \end{bmatrix}}_{Z_{\text{fault}}} \begin{bmatrix} \frac{1\angle 10}{0.06+j0.2} \\ \frac{1}{0.06+j0.2} \\ \overline{I}_3 \\ 0 \end{bmatrix} \tag{7}$$

To calculate the Thévenin equivalent of the system, we find the impedance matrix, $Z_{\text{bus}} = Y_{\text{bus}}^{-1}$. The two impedance matrices (pre-fault and fault) are shown in Eq. (6) and Eq. (7). We denote the Z_{bus} matrix before the fault by Z_{pre} and the matrix during fault by Z_{fault}. $Z_{3,3}$ is the Thévenin equivalent impedance viewed from Bus 3.

The Thévenin equivalent voltage of the system can be calculated from expanding the third row of Eq. (6) and Eq. (7):

$$\overline{V}_3 = \underbrace{Z_{31}\frac{\overline{E}_1}{Z_1} + Z_{32}\frac{\overline{E}_2}{Z_2}}_{\overline{V}_{TH}} + Z_{33}\overline{I}_3. \tag{8}$$

where, $\overline{E}_1$, $\overline{E}_2$ are the source voltage phasors and Z_1, Z_2 are the source impedances connected to Bus 1 and Bus 2 respectively.

The expression of Bus 3's voltage is shown as follows for the pre-fault and fault conditions:

$$\overline{V}_3 = (0.06 + j0.2)\overline{I_3} + 0.9962\angle 5^\circ \tag{9}$$

$$\overline{V}_3 = (0.0431 + j0.1606)\overline{I_3} + 0.5912\angle 9.5^\circ \tag{10}$$

B. Open-circuit and short-circuit tests

The above results will be further validated using the expriment measurement of the 4-bus system. To create the measurement testbeds, we modify the 4-bus system shown in Fig. 1(a), into two testbeds: one with Bus 3 as open circuit (testbed 1) and one with bus 3 as short circuit (testbed 2). Bus 3's voltage is measured in testbed 1. Additionally, the short circuit current from Bus 3 to ground is measured for the testbed 2. It can be seen that:

$$Z_{\text{TH}} = \frac{\overline{V}_{\text{OC}}}{\overline{I}_{SC}}. \tag{11}$$

where $\overline{V}_{\text{OC}}$ is the voltage phasor of Bus 3 measured in testbed 1 while $\overline{I}_{SC}$ is the current phasor measured in testbed 2.

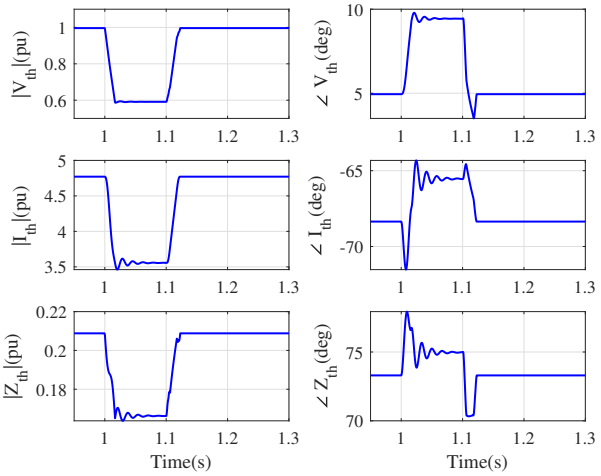


Fig. 3: The figures shows the open circuit voltage ($\overline{V}_{\text{OC}}$) and short circuit current ($\overline{I}_{\text{SC}}$) plot at Bus 3. The Thévenin equivalent impedance plot is calculated from the ratio of ($\overline{V}_{\text{OC}}$) and ($\overline{I}_{\text{SC}}$) and is presented in the 3rd row.

Fig. 3 shows the measurement data from the two testbeds showing the open-circuit voltage and short-circuit current. The Thévenin equivalent impedance plot is built using Eq. (11). The measurement is done at Bus 3, with a 3-phase fault at Bus 4 started at 1 sec and lasted for 6 cycles.

From the calculation in Eq. (9), the pre-fault Thévenin equivalent voltage is $0.9962\angle 5^\circ$ and Thévenin equivalent impedance is $0.208\angle 73.3^\circ$. The result can be validated from the measurement in Fig. 3. Similarly, Eq. (10) shows the Thévenin equivalent voltage and impedance during the 3-phase fault and indicates that the Thévenin equivalent voltage drops to 60%. The result has been be validated by Fig. 3.

IV. Fault Responses and Comparison of the Two Circuits

A major advantage of a Thévenin equivalent model is, we can simplify a bigger system. To demonstrate the advantage, two case studies are performed. The testbeds used for the experiments are shown in Fig. 4. We will show a comparison of the IBR response when IBR is connected to a 4-bus system and is connected to its Thévenin equivalent.

A. Three-phase fault

A three-phase fault will be simulated in the 4-bus system. In the single-IBR infinite-bus system, the Thévenin equivalent of pre-fault condition and during fault condition will be switched upon fault inception and fault clearance.

Eqs. (9) and (10) show the Thévenin equivalent circuits. During the normal operation the Thévenin equivalent voltage is found to be $0.9962\angle 5°$, and during the fault operation, the Thévenin equivalent voltage is found to be $0.5902\angle 9.4934°$. Fig. 4 shows the phasor diagram relating the POI voltage and the IBR's dq-axis currents during a voltage dip. This phasor digram is adapted from the one in [9] and it can be seen that upon a fault in the grid, the IBR's POI voltage experience phase jump. In turn, PLL will follow the angle jump.

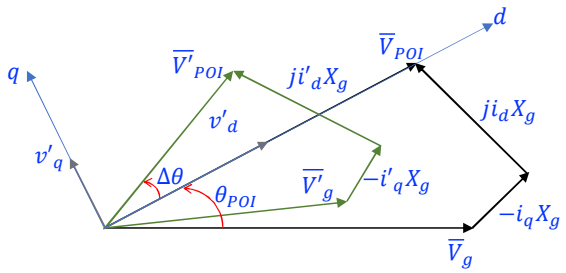


Fig. 4: Phasor diagram from grid bus to POI bus with reference to the Thévenin equivalent circuit shown in Fig. 1(b).

The responses of the IBR during the 3-phase fault can be seen in Fig. 5. It can be seen that the Thévenin equivalent can well represent the grid. The IBR performance in the two testbeds (the 4-bus system and the simplified Thévenin equivalent representation for the grid) is very similar. While there is slight difference from 1s to 1.01s in power, current and voltage measurements due to the equivalent circuit not taking into consideration in the fast transients in impedance, the angle measurements agree with each other very well. This shows that a Thévenin equivalent representation for the grid is sufficient to study PLL's behavior.

B. An SLG fault

An SLG fault is also tested. SLG faults are the most common type of fault in a power system. This is a type of unbalanced fault, meaning that the system will show the presence of positive, negative, and zero sequence components.

To generate the scenario, an A-G fault is applied on Bus 4 with a fault impedance of $j0.1$ at 1 second. For this testbed, the three phases are decoupled. Therefore, we can create the

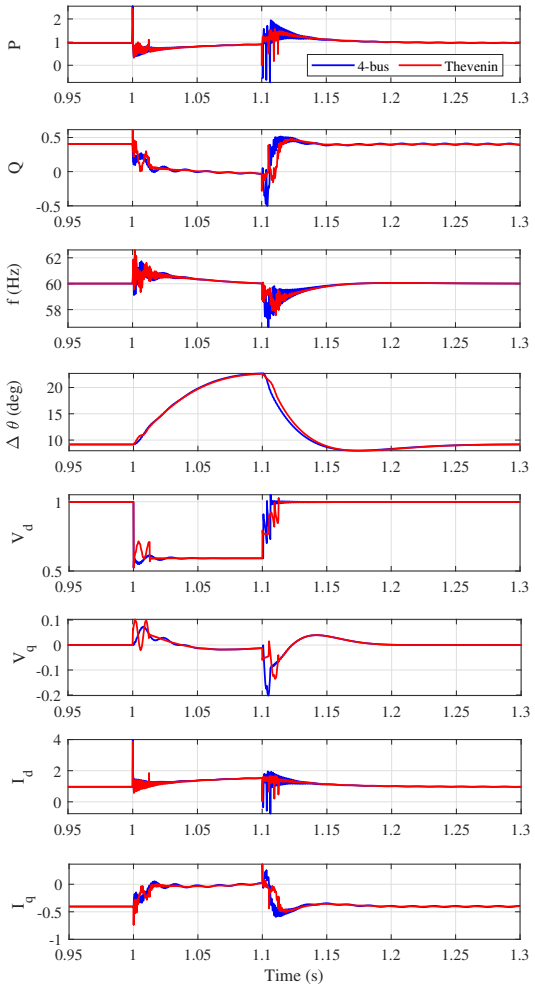


Fig. 5: Comparison of the results from bus 3 for 4-bus system and Thévenin equivalent model with IBR connected at bus 3 and three-phase balanced fault at bus 4.

Thévenin equivalent circuit for phase A from Eq. (10), and the Thévenin equivalent circuit for phase B and C can be derived from Eq. (9).

$$\overline{V}_{\mathrm{A,TH}} = \begin{cases} 0.9962\angle 5° & \text{for } t < 1s \\ 0.5902\angle 9.4934° & \text{for } 1s < t < 1.1s \end{cases}, \tag{12}$$

$$\overline{V}_{\mathrm{B,TH}} = \begin{cases} 0.9962\angle -115° & \text{for } t < 1s \\ 0.9962\angle -115° & \text{for } 1s < t < 1.1s \end{cases}, \tag{13}$$

$$\overline{V}_{\mathrm{C,TH}} = \begin{cases} 0.9962\angle 125° & \text{for } t < 1s \\ 0.9962\angle 125° & \text{for } 1s < t < 1.1s \end{cases}. \tag{14}$$

During the SLG fault, we can see an unbalanced voltage dip in phase A, which injects a positive, negative, and zero sequence components into the system. Using the Thévenin equivalent parameters from Eqs. (12) to (14), we built the Thévenin equivalent circuit with IBR connected to the system on bus 3. Since the system is under unbalanced voltage dip, the system will experience second harmonics in dq frame, which

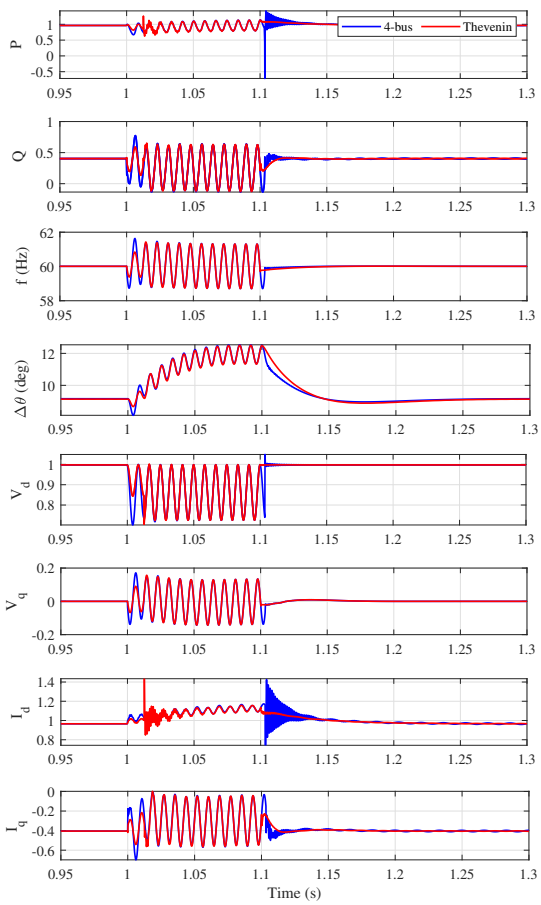


Fig. 6: Comparison of the results for the 4-bus system and Thévenin equivalent model with IBR connected at Bus 3 and an SLG fault at bus 4.

will also be seen in the power and frequency plots. The results from the two test circuits show a very good match. Also Fig. 7 shows the comparison of positive, negative and zero sequence voltage and current plot for both Thévenin equivalent and the 4-bus system.

V. Conclusion

This paper examines bus impedance matrix of a meshed network with and without fault and shows that fault conditions can be reflected in a single-IBR infinite-bus system by subjecting the grid voltage to a dip and tuning the grid impedance. The paper compares a meshed network against a single-IBR infinite-bus representation. The comparison of fault responses of IBRs shows that the PLL angle response predicted by the Thévnin equivalent circuit representation is very accurate. On the other hand, for the initial 10 ms fast dynamics, the simplified representation leads to discrepancy.

VI. Acknowledgement

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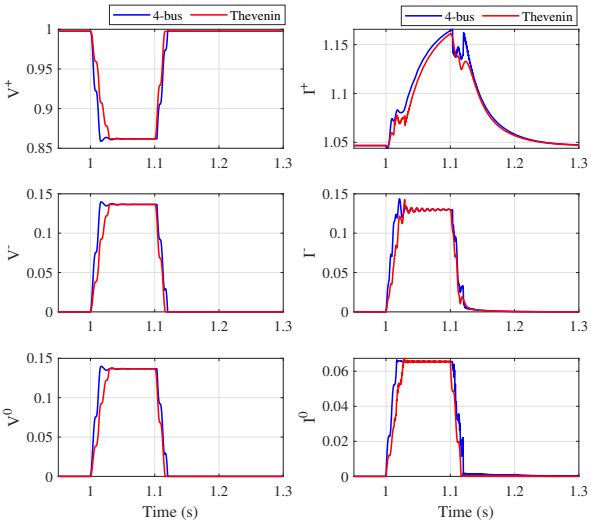

Fig. 7: Comparision of positive, negative, and zero sequence voltage and current plot for 4 bus system and Thévenin equivalent model.

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