A Novel Design for Switchable Grid-Following and Grid-Forming Control

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***Abstract*—This paper presents the design of a novel grid-forming (GFM) control structure adapted from a typical grid-following (GFL) control structure with minimal edits, thereby enabling a switchable control structure for voltage sourced converters (VSCs) to operate in either GFL or GFM mode by simply switching a flag manually. The VSC is shown to be able to operate in the GFL control mode synchronizing to the main grid through a phase-locked-loop (PLL) and operate as a GFM controller with power-based synchronization for both grid-connected and islanded conditions. To guarantee smooth operation, the control schemes and the mode switching logic have been carefully designed and examined via a series of experiments. The experiment results show that the switchable control structure can fulfill the desired control and operation functions and enable smooth transition between control modes.**

***Index Terms*—Voltage sourced converters, grid-following, grid-forming, synchronization, islanding, grid integration.**

I. Introduction

THREE-phase voltage-sourced converters (VSCs) are increasingly useful in modern power systems. An important application for VSCs is inverter-based resources (IBRs), e.g., solar photovoltaic (PV) and wind turbines [1], [2].

Control design for VSC is essential for IBRs to achieve desired functionalities for microgrid operation or grid-connected operation. In the past decade, significant progress has been made in VSC control design to suite the needs of various operational requirements. The state-of-the-art VSC control includes both the grid-following control (GFL) based on PLL and the grid-forming control (GFM) based on a controlled frequency [1]. In real-world bulk power grid operation, it has been found that PLL-synchronized GFL introduces many operational issues, including large angle deviation upon grid disturbances [3], [4], and weak grid stability issues [5], [6]. The latter issues have also been identified for VSC-HVDC operating in weak AC grids [7] in the 2000s.

The grid industry has put efforts in pushing for more GFM into the bulk power grids to have IBRs provide necessary frequency and voltage support [8]. In turn, quite a few new designs of GFM have been proposed, including single-loop control to directly control the converter's output voltage and its angle to emulate a synchronous generator [9], [10] and multi-loop control consisting of inner current control and outer control to regulate the point of common coupling (PCC) bus voltage [11], [12]. The latter structure has been adopted by the MIGRATE project for GFM evaluation in bulk power system operation [12]. The multi-loop control has a similar cascaded structure as that of the GFM in [1]. The aforementioned GFM control structures are different from a GFL in synchronization methods, where the synchronization angle is generated by a power-based control, instead of the voltage-based method (e.g., PLL). This difference has been recognized by the research community [13], [14], the National Renewable Energy Laboratory's GFM roadmap report [15], as well as the grid industry [8]. In terms of power-based synchronization, there are multiple variations, including power-frequency droop [9] and virtual synchronous generator with inertia emulated [16].

It has to be noted that while both the GFL and the multi-loop GFM employ inner current control, their outer controls are very different. The outer control of a GFL generates the current orders for the inverter's output currents, while the outer control of a multi-loop GFM [1], [11], [12] generates the orders for the shunt capacitor filter's currents, which have to be compensated by feed-forwarding the external current to further produce the inverter current orders. It can be seen that such GFM requires an additional current sensor. Additionally, the GFM's outer control regulates the PCC bus voltage by the d-axis control while the q-axis control enforces the PCC bus voltage space vector to be aligned with the synchronizing frame. This is to be compared with the voltage control in the GFL, which is realized by the q-axis outer control.

A. Motivation

The objective of this research is to design a converter controller and implement it in a chip. To make sure that the customers receive maximum benefits, the controller chip has been designed so that it can be used as either GFL (voltage-based synchronization) or GFM (power-based synchronization). To do so, we make sure that the hardware parts of the GFL and GFM are the same and the software controllers share common parts as much as possible. In this case, both GFL and GFM use the same sets of sensors, and share the current controllers.

B. Research goals

This research has two goals: 1) a switchable VSC with both GFL and GFM functions; and 2) the GFM design with the capability of seamless operational condition transition between grid-connected and standalone.

To date, the majority of the IBRs are either in GFL control mode or GFM control mode. In this research, we aim to

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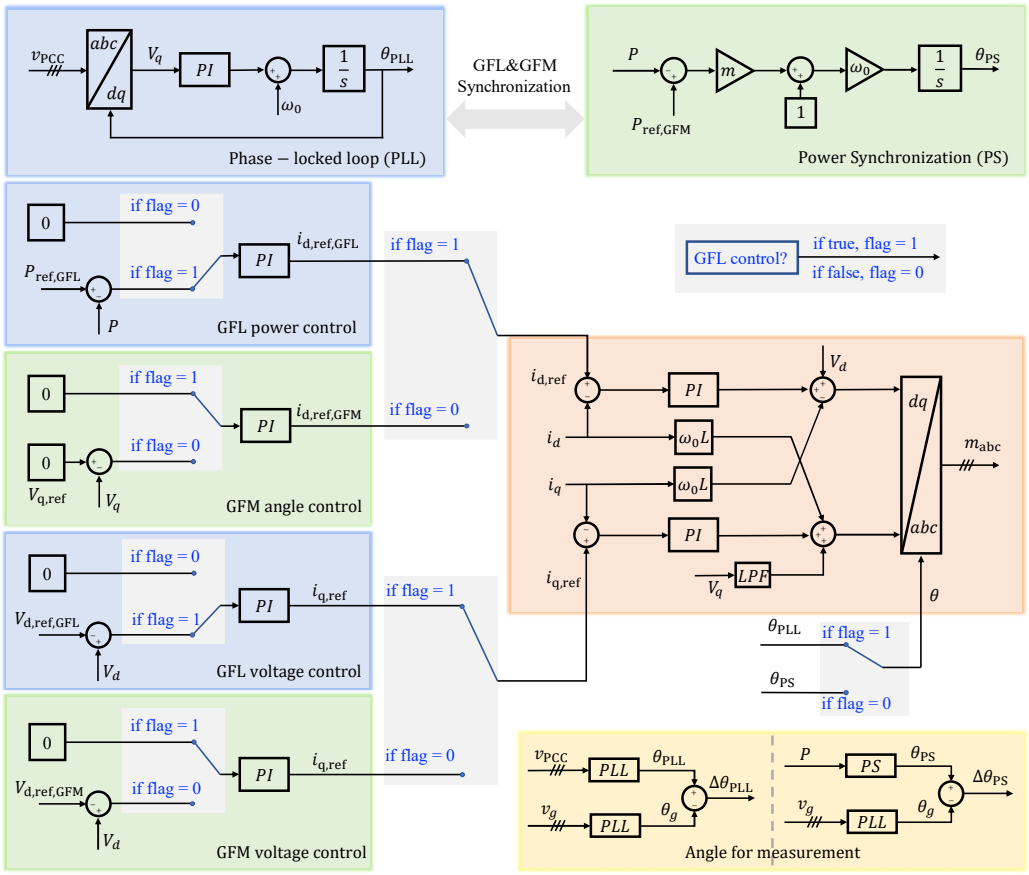


Fig. 1: The GFL and GFM switchable control strategy.

have both GFL control and GFM control in a single VSC controller chip. A selection of GFL or GFM can be realized manually by simply pressing a button. The GFL and GFM controls are based on the same two sensors: the converter's exporting current and the PCC bus voltage. A selection of GFL or GFM can be realized by simply pressing a button. This is a cost effective approach to have a VSC control in two modes, providing more flexibility. Additionally, the control design philosophy is to minimize control structure changes for the two types of controls. To this end, the GFL and GFM will not only use the same set of measurements but also share the same the inner current control.

In a recent research article [17], Lima and Watanabe designed a hybrid converter control emulating a parallel GFL and GFM. This design is also based on the assumption that the same sensors and measurements are used for GFL and GFM. On the other hand, none of the outer controls share the same structure.

This second goal of this research is to have the GFM proposed in this paper operate robustly in both operation conditions. In the previous decade, distinct controls are switched upon operation condition change, with GFL been used for grid-connected operation while GFM been used for the standalone operation [18]–[20]. This type of switching strategies requires fast detection of operation conditions and communication. Later on, research has been developed to have one controller for both operating conditions. In [21], Delgahavi and Yazdani developed a unified control strategy for this purpose. The control is based on the controllable frequency VSC presented in [1] (chapter 9) with additional active feedback compensation and droop method. Similarly, the hybrid converter control proposed in [17] can work for both operating conditions.

In this research, the designed VSC control will be analyzed and tested using hardware experiments. Compared to the time-domain simulation based testing methods employed in [17], [21], conducting hardware experiments is a noteworthy effort to achieve high feasibility.

C. Contributions

While design, prototyping, and hardware experiments of the GFLs and the multi-loop GFM have been carried out in numerous research projects, including our own research on IBR weak grid stability demonstration and control design, e.g., [22]–[25], design, prototyping, and hardware experiments of the proposed GFM with minimal edits from GFL have not been conducted. And while its performance for grid-connected condition has been checked in computer simulation in the senior authors' new book [26] (Chapter 6), islanded operation has not been checked. The current research will give a detailed examination of this control structure, configure each parameter, and provide prototyping results and experiment results for such a GFM under various operation conditions.

The contribution of this research is threefold.

1) First, a novel GFM control structure is designed, analyzed, and tested. This GFM control structure evolves from a standard GFL control structure by using the same set of measurement sensors and utilizing the same inner current control structure and q-axis outer control

structure. Only the synchronizing unit and the d-axis outer control are re-designed. Compared to the conventional design [1], [11], [12] which is based on three sensors, the new design is based on two sensors and is apparently more economical. While the outer control in the conventional design regulates the synchronizing angle through the q-axis control or the reactive current, the proposed design regulates the synchronizing angle through the d-axis control or real current while regulates voltage through the q-axis control or reactive current.

2) Second, the novel GFM control allows the manufacturing of a the switchable GFL-GFM control (including not only controllers for two modes but also switching logics). The switchable GFL-GFM has been designed, prototyped, and shown to function as desired in a hardware testbed. This proves the feasibility of the design, implicating a high practical value.
3) Third, this research not only shows results from a set of experiments but also reveals the critical difference of GFL and GFM that has not been captured in the current literature. This critical difference can be summarized as the difference of the relative position between the PCC bus voltage vector and the synchronizing frame. It plays a key role in creating different dynamic performance of GFL and GFM, as shown in the experiment results.

D. Structure of the paper

The sections following outline the switchable VSC control design, analysis, hardware setup, and experiment results. The switchable control design is presented in Section II. The hardware testbed setup is then presented in Section III. Section IV presents four sets of experiment results, including basic control function tests, control mode switching tests, operating condition switching tests, and grid voltage dip tests, along with detailed insightful analysis. Finally, Section V summarizes this paper and highlights the contributions.

II. Switchable VSC Control

Fig. 1 shows the switchable VSC control. The VSC can operate in the GFL mode when the flag is set to 1 and operate in the GFM mode when the flag is set to 0. The figure shows that there are two different outer controls that generate the reference signals for the inner loop current control. The GFL control regulates real power in the d-axis and regulates AC voltage in the q-axis, while the GFM control enforces the alignment of the PCC bus voltage with the synchronizing frame in the d-axis and regulates the AC voltage in the q-axis.

Aside from the difference in d-axis outer control, the main difference between GFL and GFM is the synchronization method. In GFL, voltage-based synchronization or PLL is used to generate a synchronizing angle $\theta_{\rm PLL}$ while in grid-forming control, power-based synchronization is used to generate a synchronization angle $\theta_{\rm PS}$. In this paper, power-frequency droop control has been adopted as the synchronizing control. It is also easy to implement a virtual synchronous generator control with inertia emulated.

It is worthwhile to note that the GFL and the GFM use the same sensors. Compared to the conventional GFM control proposed in the literature, e.g., [1], [11], [12], the current one has a few distinct features leading to easy implementation for switchable GFL-GFM control.

- The GFM in [1], [11], [12] has its outer control's d-axis for V_d control and q-axis for V_q control. This control structure is completely different from a GFL's where q-axis is for voltage/var control.
- The GFM in [1], [11], [12] has cross coupling terms in its outer control and its outputs are the capacitor filter's current orders. On the other hand, for the inner current control, the converter current measurement is to be used. In order to generate the converter current orders, the conventional GFM requires an additional current sensor to measure the external current and feedfoward the current measurements to generate the converter current orders. This makes the GFM control quite complicated.

In short, the GFM control implemented in this paper is much simpler in structure and maximumly reuses the blocks of GFL. How to select GFL control parameters has been well studied in the past, e.g., [1]. Most recently, the per unit-based control design analysis and parameter selection have been documented in detail with each parameter given in [27]. Also, a typical number for the power-frequency droop parameter m is also well known, e.g., 3%, 5%. The parameters of the control are shown in Table I. The only challenging task is to set the parameters for the GFM's d-axis outer control. This will be presented in the following.

TABLE I: Parameters for the circuit and the VSC control.

Description	Symbols	Values (SI/pu)
Power base	S_b	20 VA
Voltage base (LL, rms)	V_b	17.32 V
System frequency	f	60 Hz
Grid voltage (LL, rms)	v_g	17.32 V
DC voltage	$V_{\rm DC}$	40 V
Switching frequency	$f_{\rm SW}$	4 kHz
Choke filter	R_f	0.0094 pu
Choke filter	L_f	0.0754 pu
Shunt C	C_f	0.2658 pu
Transmission line	R_t	0.0029 pu
Transmission line	L_t	0.2155 pu
Load resistance	R_l	1.33 pu
GFM: P-f droop gain	m	3% pu
GFL: PLL	*PI*	40+400/s
Inner current control	*PI*	0.3+20/s
GFL power control	*PI*	0.6+60/s
GFL voltage control	*PI*	0.4+40/s
GFM angle control	*PI*	2+14/s
GFM voltage control	*PI*	3+40/s

A. Philosophy of the d-axis angle control for GFM

The design of the d-axis outer control for GFM is based on the grid-operating condition with the grid been treated as a constant voltage source behind a pure reactance jX, while the VSC is treated as a current source synchronized to the grid through a synchronizing angle δ. This treatment is reasonable since the inner current control is very fast compared to the outer control. This circuit topology is illustrated in Fig. 2.

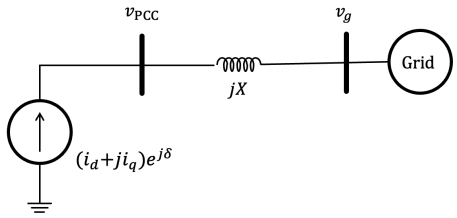


Fig. 2: Illustrative circuit of an IBR integrated to a grid.

The PCC bus voltage and the current viewed from the grid dq-frame is as follows.

$$\overline{V} = Ve^{j\delta_{\text{PCC}}} = jX(i_d + ji_q)e^{j\delta} + \overline{V_g}, \tag{1}$$

where δ is the relative angle of the synchronizing frame against the grid. Hence δ is either $\Delta\theta_{\text{PLL}}$ or $\Delta\theta_{\text{PS}}$. The grid impedance is assumed purely reactive and the reactance is X. If the grid dq-frame is aligned with the PCC bus voltage space vector at the initial steady state, then δ_{PCC} and δ are 0 initially. The small-signal relationship of the above equation is:

$$\Delta V + jV\Delta\delta_{\text{PCC}} = jX\left((\Delta i_d + j\Delta i_q) + j\overline{I}'\Delta\delta\right), \tag{2}$$

where $\overline{I}' = i_d + ji_q$ is the initial current vector viewed from the synchronizing frame. The imaginary part of Eq. (2) is:

$$V\Delta\delta_{\text{PCC}} = X\Delta i_d - Xi_q\Delta\delta \approx X\Delta i_d, \text{ if } i_q \text{ is small.} \tag{3}$$

Eq. (3) shows that Δi_d is proportional to the PCC bus voltage angle $\Delta\delta_{\text{PCC}}$. Therefore, i_d may be adjusted to track $\Delta\delta_{\text{PCC}}$.

Note that V_q is the PCC voltage's projection to the q-axis of the synchronizing dq-frame. Hence:

$$V_q = V\sin(\delta_{\text{PCC}} - \delta) \approx \delta_{\text{PCC}} - \delta, \text{ if } V \approx 1. \tag{4}$$

With $-V_q$ or $(\delta - \delta_{\text{PCC}})$ passing into the d-axis PI controller to generate i_d order, i_d may be adjusted to further influence δ_{PCC} according to Eq. (3). Also, δ_{PCC} influences the real power exporting. Eq. (5) presents the power and angle relationship assuming the PCC voltage is kept constant at 1 pu.

$$\begin{aligned} P &= \frac{VV_g}{X}\sin\delta_{\text{PCC}}, \\ \Longrightarrow \Delta P &= \frac{\cos\delta_{\text{PCC}}}{X}\Delta\delta_{\text{PCC}}. \end{aligned} \tag{5}$$

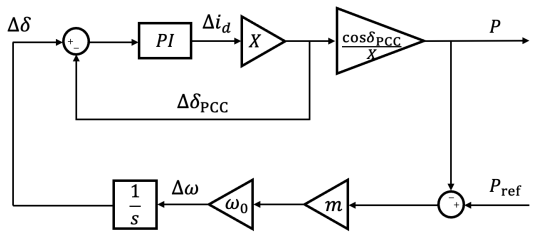


Fig. 3: The block diagram illustrates the relationship between the d-axis angle control and the power-frequency droop when the GFM is in the grid-connected condition.

Combining (3), (4), and (5), the d-axis control and the power-frequency droop control, the block diagram relating the synchronizing angle, the PCC bus angle, and real power is shown in Fig. 3.

The closed-loop transfer function from δ to δ_{PCC} becomes:

$$\frac{\Delta\delta_{\text{PCC}}}{\Delta\delta} = \frac{\Delta\theta_{\text{PCC}}}{\Delta\theta_{\text{PS}}} = \frac{X\left(K_p + \frac{K_i}{s}\right)}{1 + X\left(K_p + \frac{K_i}{s}\right)} = \frac{Ts+1}{T_1 s+1}, \tag{6}$$

where $T = K_p/K_i$ and $T_1 = T + 1/(XK_i)$, K_p and K_i are the d-axis outer control parameters.

The loop gain from the synchronizing angle $\Delta\delta$ to real power P and back to itself can be found as follows:

$$\text{Loop Gain} = \frac{Ts+1}{T_1 s+1}\frac{\cos\delta_{\text{PCC}}}{X}\frac{m\omega_0}{s}. \tag{7}$$

This feedback system is always stable under the assumption that the PCC bus voltage is well controlled. The closed-loop system from the power order to the PCC bus voltage angle is further examined. This system is presented as follows:

$$\frac{\Delta\delta_{\text{PCC}}}{\Delta P_{\text{ref}}} = \frac{T_1 s+1}{\frac{T_1}{m\omega_0}s^2 + \left(\frac{1}{m\omega_0} + \frac{\cos\delta_{\text{PCC}}}{X}T\right)s + \frac{\cos\delta_{\text{PCC}}}{X}}. \tag{8}$$

It can be seen that the closed-loop system is a second-order system. If T ($T = K_p/K_i$) is too small, the system may subject to oscillations.

Fig. 4a shows the Bode diagrams of the closed-loop system for two set of PI controllers ($2 + 14/s$ vs. $0.2 + 14/s$) under a varying grid impedance. Fig. 4b shows the time-domain response of $\Delta\delta_{\text{PCC}}$ subject to a step change in the power order. The grid impedance varies: 0.25 pu, 0.50 pu, 0.75 pu, 0.95 pu. It can be seen that $0.2 + 14/s$ may lead to a peak at about 2 Hz when X is below 0.95 Hz in the Bode diagrams, and overshoot due to oscillations at about 2 Hz in the time-domain responses. Therefore, to achieve robust performance, $2 + 14/s$ is chosen as the PI controller for the d-axis outer loop of the GFM.

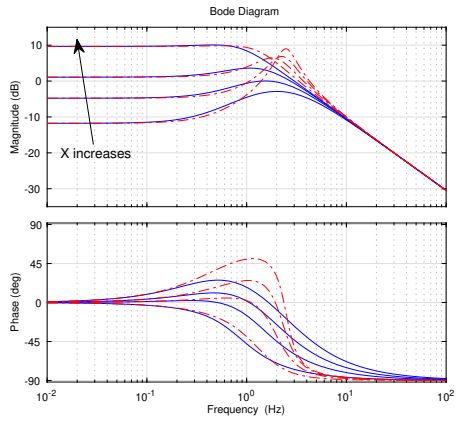
B. Analysis of the GFM control for standalone operation

While the GFM design is based on the grid-connected operating conditions, this control is also analyzed for the standalone operation when the GFM is serving a resistive load. Fig. 5 illustrates the circuit of a GFM serving a resistive load where the GFM is again treated as a controllable current source. It can be seen that the dq-frame PCC bus voltage is related to the dq-frame IBR current as follows:

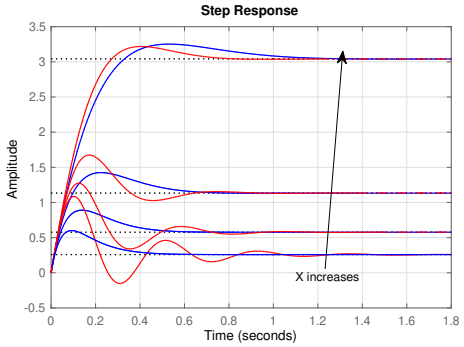
$$\Delta v_d = R_l\Delta i_d, \;\; \Delta v_q = R_l\Delta i_q. \tag{9}$$

The effect of the inner current control is modeled as a low-pass filter $1/(\tau s + 1)$. It can be seen that Δv_q is the input to the d-axis outer control influencing Δi_d, while the Δv_d is the input to the q-axis outer control influencing Δi_q. These relationships form a closed-loop system shown in Fig. 6.

In this feedback system, the q-axis voltage control needs to be tuned to coordinate with the d-axis control ($2 + 14/s$) for stability. Fig. 7 shows the open-loop system Bode diagrams for two sets of the voltage PI control: $0.4 + 40/s$ vs. $3 + 40/s$. The integral gain is 40, while the proportional gain of 0.4 and 3 are compared. The resistive load R_l is at 20 Ω or 1.33 pu and the low-pass filter's time constant is assumed to be 25 ms. The blue dotted line (when $k_p = 0.4$) in Fig. 7 shows that at 10 Hz,



(a)



(b)

Fig. 4: (a) Bode diagram of $\Delta\delta_{\mathrm{PCC}}/\Delta P_{\mathrm{ref}}$. (b) Step responses of $\Delta\delta_{\mathrm{PCC}}/\Delta P_{\mathrm{ref}}$. Blue lines: $2+14/s$. Red lines: $0.2+14/s$.

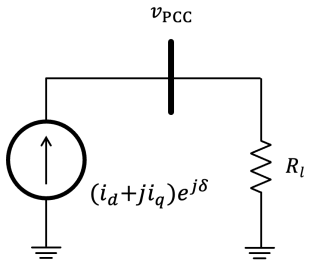


Fig. 5: The circuit of a GFM serving a resistive load R_l.

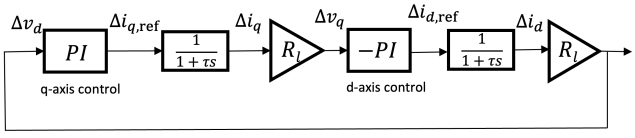


Fig. 6: The block diagram illustrates the relationship between the d-axis control and q-axis control when the GFM is in the standalone operation serving a resistive load.

the phase goes below 180 degrees, while the magnitude has a gain greater than 0 dB, implicating instability. Increasing the proportional gain helps mitigate the stability issue. Therefore, it can be seen that the voltage control's proportional gain should be increased to ensure stability.

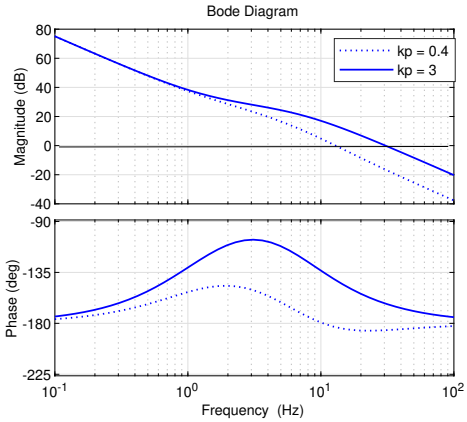
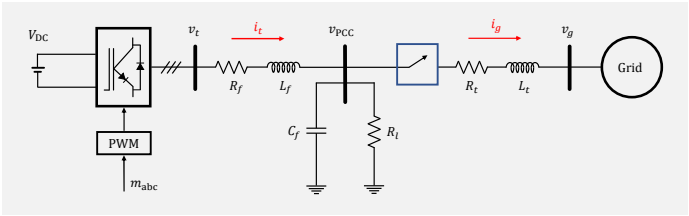
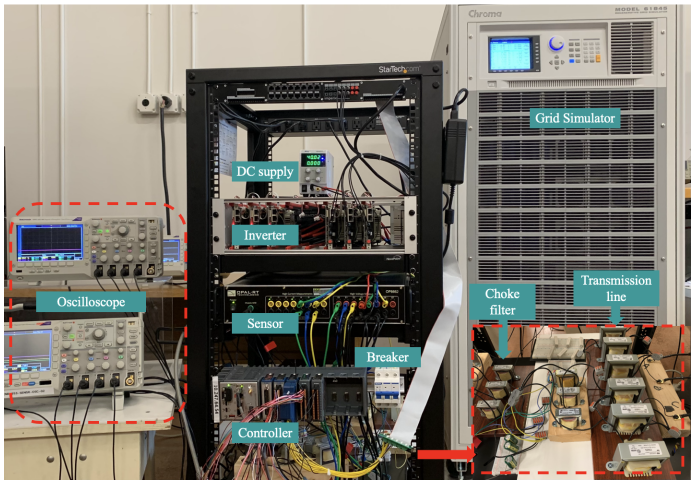


Fig. 7: The Bode diagram of the open-loop system in Fig. 6, illustrating the potential oscillatory stability issue if the voltage control's proportional gain is too small.



(a)



(b)

Fig. 8: (a) The testbed's circuit diagram. (b) The hardware setup of the testbed at the USF SPS lab.

III. The Test System and Its Hardware Setup

As illustrated in Fig. 8a, the test system is a three-phase VSC that can be operated in both islanding and grid-connected conditions. The VSC is connected to the grid via a choke filter, a shunt capacitor filter, and a transmission line. The choke filter consists of R_f, L_f while the shunt capacitor is notated as C_f. The transmission line is represented by an RL impedance consisting of resistance R_t and inductance, L_t. The flow of power is indicated by the red arrow. The grid is connected to the VSC through a switch, allowing the system to be operated in both grid-connected and islanding conditions. The PCC bus

is located between the choke filter and the transmission line, where it is also connected to a resistive load R_l. In islanding operation, the VSC serves the load only.

The circuit presented in Fig. 8a has been built as a hardware testbed, shown in Fig. 8b. The three-phase VSC is a Silicon Carbide MOSFET module which can handle up to 800 V DC, 24 A continuous current, with a maximum switching frequency of 200 kHz. The choke filter and the transmission line are represented by inductors. The shunt filter capacitor is a 400-V 47-μF capacitor. The details of the parameters are presented in Table I.

The grid is represented by the Chroma regenerative grid simulator. This device is a programmable bidirectional power supply that can operate at up to 45 kVA power and can provide a constant voltage output of 400 V per-phase with an operating frequency between 30-100 Hz. The device can be used to generate both single-phase and three-phase voltages. To switch between grid-connected and islanding conditions, we use a miniature circuit breaker (MCB), shown in both Fig. 8a and Fig. 8b.

In order to design the VSC control, we need to measure the voltage of the PCC bus and the current exporting from the VSC. The OPAL-RT voltage and current sensor, OP-8662 is used to collect measurements. This device has eight voltage sensors and eight current sensors. The voltage sensor can measure up to 600 V and the current sensor can measure up to 15 A at a sampling frequency of 100 kHz.

The most important part of this setup is the IO modules which connects the sensor to the controller. We use National Instrument (NI) 9205 as an analog input module, which is connected to the NI cRIO 9049 as the controller hardware. The voltage and current sensor modules have the ability to reduce the measured quantities to an acceptable range for the analog input module.

The cRIO 9049 is a real-time embedded industrial controller which consists of a real-time controller, reconfigurable IO Modules (RIO), FPGA module and an Ethernet expansion chassis. It is capable of real-time signal communication and control. This device runs on a 32-bit Linux real-time OS and has an FPGA module that can operate at a sampling rate of 40 MHz. This device serves as a platform for communication with the remote PC running LabVIEW software, allowing a developer to visually examine the data through NI's input and output modules and design the controller in LabVIEW. The control signal generated in LabVIEW is fed back to the inverter digital port through a digital out module. For monitoring purposes and to save the data from the testbed, we use an analog out module and feed the signal to 4 oscilloscopes.

IV. Experiment Results

Overall, three categories of tests have been conducted with the details of cases documented in Table II.

1) Category 1: Basic control function tests to confirm the VSC control can fulfill its simple control functions, e.g., power/voltage order following.
2) Category 2: GFL/GFM mode switching tests during steady-state operating or sudden islanding to examine the feasibility of the mode switching logic and the performance of the system.
3) Category 3: Grid fault tests to examine the performance of the IBR and the benefits of mode switching.

TABLE II: Lists of hardware experiments and simulation tests.

Cat	Cases	Description	Comments
1	$A1$	GFL power and voltage reference step changes	hardware
	$A2$	GFM power and voltage reference step changes	hardware
2	$B1$	Control mode switching & system condition changes	hardware
	$B2$	Sudden islanding & control mode switching	hardware & simulation
3	$C1$	Three-phase grid voltage magnitude dip	hardware & simulation
	$C2$	Weak grid event	simulation
	$C3$	Grid voltage dip, line tripping following by mode switching	simulation

It is noteworthy to point out that majority of the research papers on control and operation strategy tests rely on computer simulation only, e.g., [17], [21], [28], [29], while this research has conducted control hardware prototyping and testing in a hardware experiment testbed. Additionally, this hardware testbed has been modeled for computer simulation. The hardware and the electromagnetic transient (EMT) simulation testbeds have been benchmarked.

A. Category 1: Basic control function tests

The control strategy built in LabVIEW is capable of operating in both GFL and GFM controls by the toggle of a switch. In this section, we validate the successful operation of the individual control mode by giving a step change in the control commands.

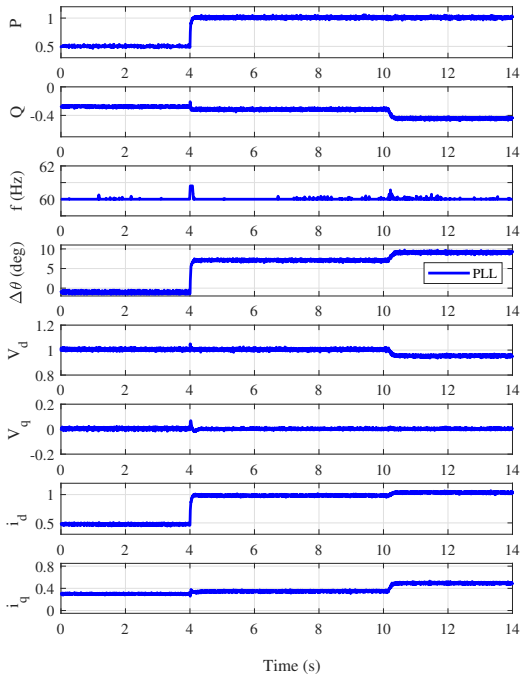
1) A1: GFL: When the system is operating in the GFL mode, a PLL is used to synchronize the inverter with the grid. In addition, real power and PCC bus voltage are regulated through the inverter's outer control. To run the testbed in the grid-following control mode, we set the flag as 1 or GFL control mode. The inner current control's commands $i_{\mathrm{dq,ref}}$ are generated from the real-power and AC voltage regulators.

Two consecutive experiments were conducted to test the basic control functions of GFL. Initially, the inverter is sending out 0.5 pu real power and the PCC voltage is 1 pu.

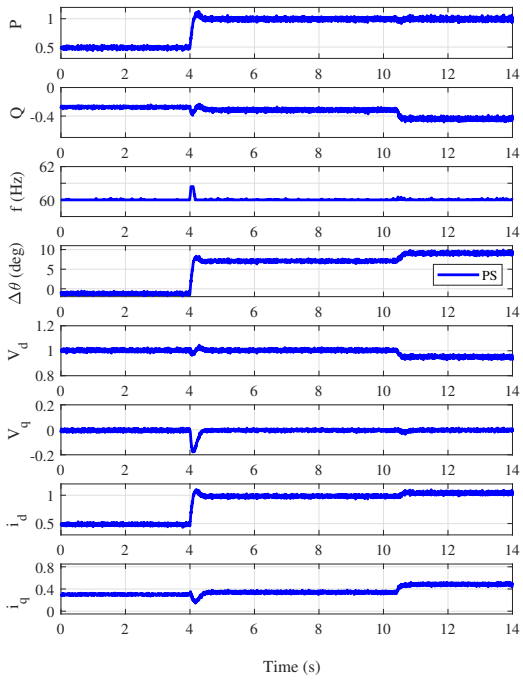
- At $t = 4$ s, $P_{\mathrm{ref,GFL}}$ is subject to a step change to increase its value from 0.5 pu to 1.0 pu.
- At $t = 10.1$ s, $V_{\mathrm{d,ref}}$ is subject to a step change to decrease its order from 1 pu to 0.95 pu.

A series of measurements are taken, including the real power and reactive power from the converter to the grid measured at the PCC bus, the frequency and angle output of the PLL, the dq voltage and current components in the PLL frame. Note that the PLL's angle is a relative angle against a synchronous rotating frame. This frame aligns with the PLL frame before 4 s.

Fig. 9a shows experiment results of the testbed. It can be seen that the real power measurement follows the real power command to increase from 0.5 pu to 1.0 pu after 4 s; the AC



(a)



(b)

Fig. 9: Cases A1 and A2: Hardware experiment results. Basic control function tests for a step change in real power order from 0.5 to 1 pu at 4 s and a step change in V_d order from 1 to 0.95 pu at 10 s. (a) GFL; (b) GFM.

voltage measurement (V_d based on the PLL frame) follows the command to decrease from 1.0 pu to 0.95 pu after 10.1 s.

Since the control uses PLL-based voltage synchronization, the q-axis voltage of the PCC bus is forced to be zero. It can be seen that V_q based on the PLL frame is 0 all the time, except small transients during the command change instants. Before 10.1 s, the PCC bus voltage is kept at 1 pu. The real power and the reactive are associated with the dq-axis currents as follows:

$$P = V_d i_d, \;\; Q = -V_d i_q. \tag{10}$$

It can be seen that i_d is indeed 0.5 pu before 4 s and 1.0 pu after 4 s. After 10.1 s, since the PCC voltage reduces, to maintain the same level of real power, i_d should increase. This is also reflected in the experiment results of i_d measurement. Research conducted in [30] has shown that the PCC bus' voltage phase angle is proportional to i_d. Since PLL's angle tracks the PCC bus' voltage phase angle, hence, the PLL angle increases if i_d increases. It can be seen that the trajectory of the PLL angle is similar as that of i_d.

Additionally, based on the change in the angle (about 7 degrees due to 0.5 pu power increase), we may estimate the total transmission line reactance X.

$$\Delta P = \frac{1}{X}\Delta\theta, \Longrightarrow X = \frac{7 \times \frac{\pi}{180}}{0.5} = 0.2443. \tag{11}$$

We can see that this number is slightly larger than the name plate number from the inductor. Similarly, the change in the voltage and the change i_q has the following relationship:

$$\Delta V \approx -X\Delta i_q. \tag{12}$$

When the voltage reduces by 0.05 pu, i_q increase by 0.2 pu. This implicates that X is approximately 0.25 pu.

Overall, the basic control functions can be fulfilled and the IBR behaves as expected.

2) A2: GFM: Fig. 9b shows the test results of the GFM control. GFM adopts power-based synchronization. Eq. (13) shows the droop relationship used to generate frequency, where m is the droop gain notating the change of frequency in pu vs. the change of power in pu.

$$\omega - \omega_0 = m\,\omega_0\,(P_{\text{ref,GFM}} - P) \tag{13}$$

The GFM control can be used for both grid-connected and islanding modes.Under grid-connected mode, the frequency will be synchronized with the grid $\omega = \omega_0$, hence the power measurement P should track its order $P_{\text{ref,GFM}}$ at steady state.

To test the basic control functions of the GFM, we conducted two consecutive experiments.

- At $t = 4$ s, $P_{\text{ref,GFM}}$ increases from 0.5 pu to 1.0 pu.
- At $t = 10.1$ s, $V_{\text{d,ref}}$ decreases from 1.0 pu to 0.95 pu.

The dq voltage and current components are all based on the GFM's synchronization frame. It can be seen that the d-axis outer control functions properly by keeping V_q at 0 for all the time. The P-f droop control functions properly to keep the difference between the power order and the power measurement at 0. The power measurement can track the power order at 4 s. V_d is kept at 1 pu before 10.1 s and follows the order to be 0.95 pu.

3) Analysis: Comparison of GFL and GFM: While all the rest of signals behave very similar as their counterparts in the GFL control case, V_q is shown to have different transients upon power order increase. In the GFL case, V_q has a negligible upward spike at $t = 4$ s while in the GFM case, V_q has an obvious downward spike. The two types of spikes are explained in Fig. 10 and also as follows.

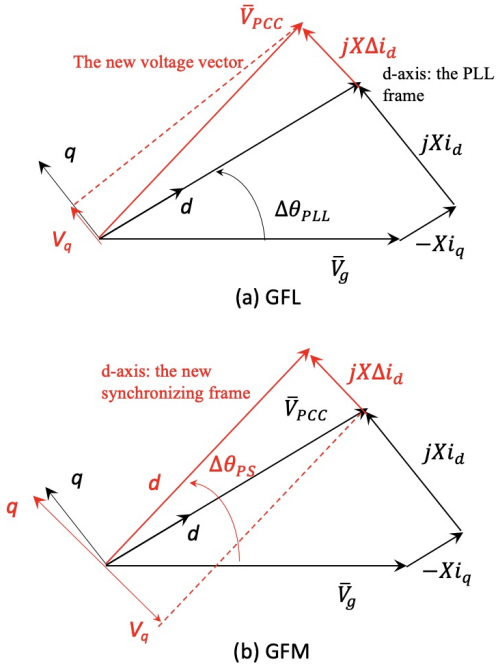


Fig. 10: The positions of the PCC bus voltage vector vs. the synchronization frame upon a step increase in the power order. Red color notates the variables subject to immediate change. (a) GFL. (b) GFM.

In the GFL case, upon the power order increase, the d-axis current order increases due to the power control logic and in turn the d-axis current measurement increases. This increase is also reflected in the increase in the PCC bus voltage angle, since i_d influences the angle according to Eq. (3). V_q in the PLL frame then experiences an increase since the PCC bus voltage vector leads the PLL frame. The PLL's PI controller follows up and enforces V_q to be 0. Hence, an upward spike is seen.

In the GFM case, upon the power order change, the synchronization angle increases immediately due to the power-frequency droop based synchronization control. The PCC bus voltage vector is initially aligned with the synchronization frame. Upon the sudden power order increase it is now lagging the synchronizing frame, resulting in its q-axis projection to the synchronizing frame becoming negative while its d-axis projection decreases. The d-axis outer control then brings V_q back to 0, or realign the PCC bus voltage to the new synchronization frame. This is achieved by increasing i_d. Therefore, V_q shows a downward spike upon the power order step change.

Remarks: The difference of the synchronization methods of GFL and GFM leads to the difference in the relative position of the PCC bus voltage vector vs. the synchronization frame. Upon the power order increase, in GFL the PCC bus voltage vector has an immediate increase in its angle while in GFM the synchronization frame has its angle immediately increased. In turn, in GFL the synchronization frame lags the voltage vector while in GFM the synchronization frame leads the voltage vector.

Overall, the GFM can fulfill its control functions and behaves as expected.

B. Category 2: GFL/GFM mode switching

It has to be noted that control mode switching during operation is manually conducted by the system operators. It is not the intention of this paper to develop an automatically triggered control mode switching strategy. Control mode switching will be executed by system operators. They will make necessary observation before executing control mode switching to avoid large transients. For example, while switching for the first time between GFL and GFM, it is necessary to observe the difference in angle between voltage synchronization and power synchronization. The switching has to be triggered at a minimum angle difference, to avoid a big transient or even unstable condition.

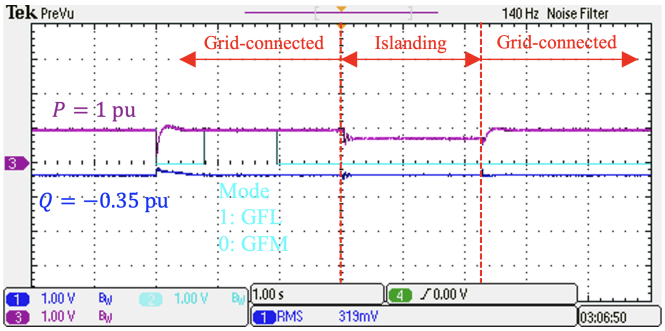
1) Case B1: Control mode switching and system condition switching: GFL and GFM mode switching and operational condition switching between grid-connected and islanding have been tested. The event sequence is shown in Fig. 12a, while the experiment results shown in Figs. 11 and 12b. Note that the dq components are based on the synchronizing frame. When GFL is enabled, this frame is the PLL frame. When GFM is enabled, this frame is the power synchronization angle based frame.

Fig. 11 shows the experiment results from the four oscilloscopes where each measurement has a distinct scale and it is difficult to compare a current order vs. a current measurement. Hence, the signals are replotted in Fig. 12 to group similar signals together using the same scale. The operation panel designed in LabVIEW. GFL and GFM mode switching can be done by pushing a button in the front panel, while the operational condition can be changed by physically switching the breaker in the testbed.

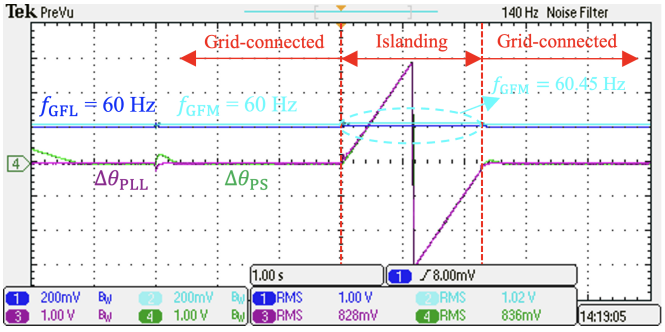
a) Case B1 stage 1: control mode switching: From 0 s to 5 s, the VSC is operating to be connected to a grid. When the control mode toggles between GFL and GFM, the d-axis current order and the synchronization angle have to be switched from GFL's to GFM's. Additionally, when either one control block in GFL (or GFM) is enabled, it is desirable to keep its counter part in GFM (or GFL) disabled, or the output of the block remains intact. Therefore, the input to the PI controller of the outer loop is subject to the mode change. If the GFL is enabled, the real power control has the power error as the input while the GFM's angle control or V_q control has its input set to 0. If GFM is enabled, the GFL's real power control then has its input switched to 0 while the GFM's V_q control has its input as the V_q error.

During the control mode switching, if the system's operating point (e.g., real power, voltage) does not change, a very smooth transition can be achieved.

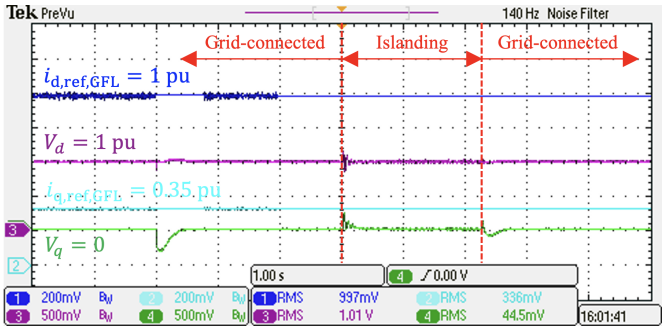
Fig. 11 and Fig. 12b present the experiments results from the hardware testbed, showing the switching between different modes at the grid-connected condition from 0 s- 5 s. Initially the VSC is in GFL control mode. At $t = 2$ s, the mode is switched from GFL to GFM and there are some transients. This is due to the initial setting. When the test bed is energized, the VSC is in the GFL control mode with the GFM control



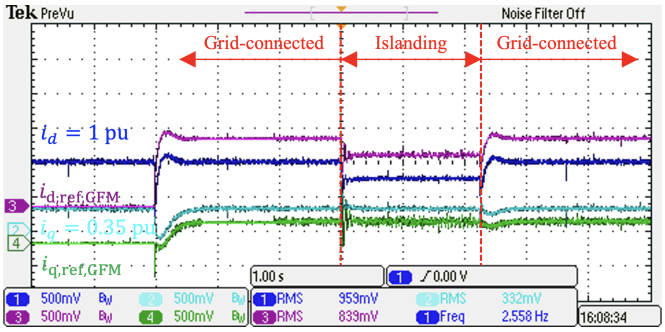
(a) Reactive Power (blue), Switch indicator (Cyan) and Real Power (purple).



(b) f_{GFM} (blue), f_{GFL} (cyan), θ_{GFL} (purple) and θ_{GFM} (green).



(c) $i_{\mathrm{d,ref,GFL}}$ (blue), $i_{\mathrm{q,ref,GFL}}$ (cyan), V_d (purple), V_q (green).



(d) i_d (blue), i_q (cyan), $i_{\mathrm{d,ref,GFM}}$ (purple), $i_{\mathrm{q,ref,GFM}}$ (green).

Fig. 11: Case B1: display in four oscilloscopes. The system runs initially in GFL control. It switches from GFL to GFM at 2 s, back to GFL at 2.8 s, and finally GFM after 4 s. The testbed is operating in the grid connected mode before 5 s while in the islanding mode after 5 s. Note each signal has a distinct scale making comparison slightly difficult.

in the off mode. Hence, when the GFM is enabled, its dq-axis current order $i_{\mathrm{d,ref,GFM}}$ is 0 and this results in the dq current and the real and reactive power measurements moving towards 0 at the instant of switching. The reduction of the real power measurement makes the power synchronization unit to have an increased frequency and a synchronizing angle. Hence, in Fig. 11b, $\Delta\theta_{\mathrm{PS}}$ is seen to have an upward spike. This then leads to a decrease in V_q since now the PCC bus voltage vector is lagging the synchronizing frame based on Fig. 10. In turn, $i_{\mathrm{d,ref,GFM}}$ increases based on the d-axis outer control logic and i_d follows the order and becomes 1 pu. Before $t = 2$ s, the VSC is absorbing 0.35 pu reactive power. At the moment of switching from GFL to GFM, the reactive power increases, leading to an increased voltage magnitude V_d. The q-axis outer control works to bring the voltage back to 1 pu by increasing the q-axis current reference $i_{\mathrm{d,ref,GFM}}$ and in turn i_q. In about 0.5 seconds, a new steady state is achieved for all measurements.

In the next two mode switching events at 2.8 s and 4 s, since the operating condition does not change at all, the switching transients are negligible. It is also interesting to point out at $t = 2$ s, when the new synchronization angle based on power measurement increased, in turn the PCC bus voltage vector also experiences an increase in angle. Viewed from the PLL frame, the voltage vector has its q-axis projection decreases and hence the PLL shows a downward spike in its frequency. Hence, in Fig. 12b's frequency plot, the dynamics of the frequency measurements from the GFL and the GFM have opposite trends.

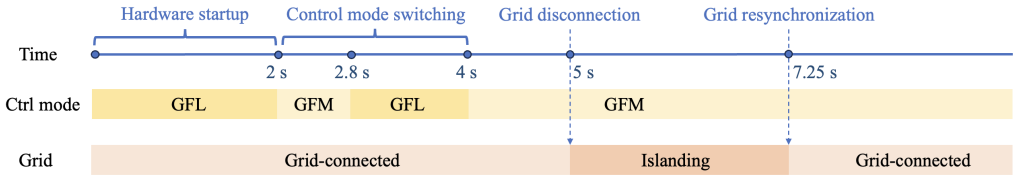
Fig. 13 is the zoomed-in version of Fig. 12b from 2.5 s to 4.5 s. It can be seen that the current order transients are very smooth, while there is discernible difference in ripples from one mode to another mode.

b) Case B1 stage 2: operation condition switching: At $t = 5$ s, while the VSC is running in GFM control, the system is switched to the islanding condition by switching off the breaker manually thereby disconnecting the grid. The experiment results from 5 s to 7.25 s shown in Fig. 11 and Fig. 12b are for the islanding condition. From 7.25 s to 10 s, the operating condition is back to the grid-connected condition. The system is operating smoothly for the condition switching. In islanding operation from 5 s to 7.25 s, the power reference is 1 pu while the load consumes 0.75 pu. In turn, the microgrid's frequency rises to 60.45 Hz based on 3% P-f droop parameter:

$$\Delta f = -(0.75 - 1) \times 3\% \times 60 \text{ Hz} = 0.45 \text{ Hz}. \quad (14)$$

The relative angle against the grid should keep increasing. Both the frequency and the angle responses in Fig. 12b show the expected responses.

At $t = 7.25$ s, the breaker is again manually switched on and thereby the VSC is reconnecting to the grid. It has to be mentioned that the angle between the synchronizing frame and the grid ($\Delta\theta_{\mathrm{PS}}$) is monitored closely. Only when this angle is close to 0, the switching on action is initiated. This makes sure that at that moment, the PCC voltage space vector almost aligns with the grid voltage space vector even their rotating speeds (frequencies) are different. The resulting transient is minimized. It can be seen upon the breaker switching on, the angle immediate stops increasing and stays at a constant value after a quick transient. The dq-axis voltages also show very smooth transients.



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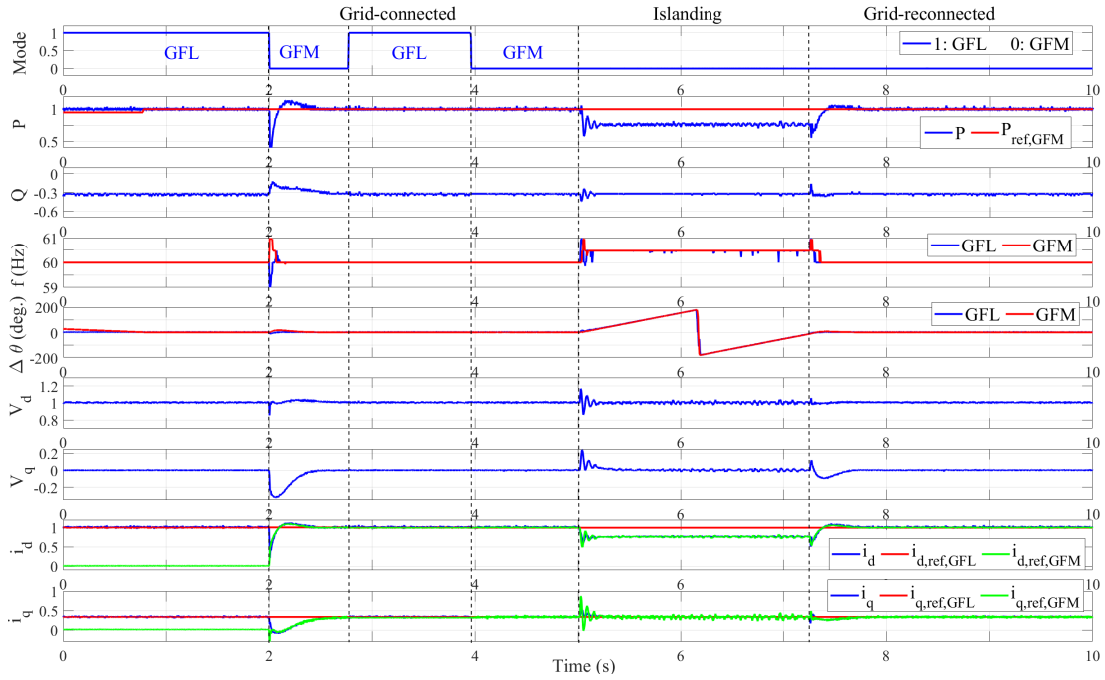


(b)

Fig. 12: Case B1. (a) Sequence of the events. (b) The experiment results based on data extracted from the oscilloscope results shown in Fig. 11.

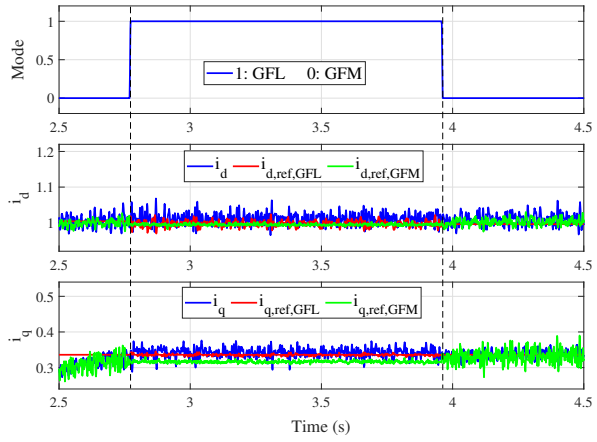


Fig. 13: Smooth switching from GFL to GFM and vice versa.

In short, the GFM control is capable to operate in both grid-connected and islanding conditions.

2) Case B2: Sudden Islanding: Fig. 14 shows the event sequence. Initially, the grid-connected system was operating in the GFL control mode. The grid was disconnected at 0.5 seconds. The frequency sensed by the PLL of the IBR will be increase rapidly and exceed the normal range of 59 Hz to 61 Hz. Therefore, the control system will be notified to switch to GFM control mode with a delay of 6 cycles. This delay emulates the communication delay between the sensor and a controller. The hardware experiment results of the system with/without control switching protection are shown in Fig. 15.

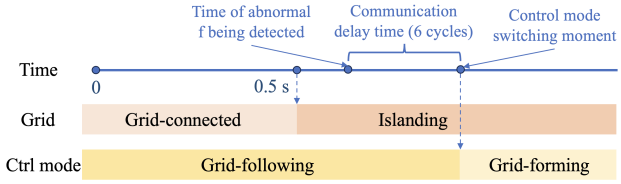
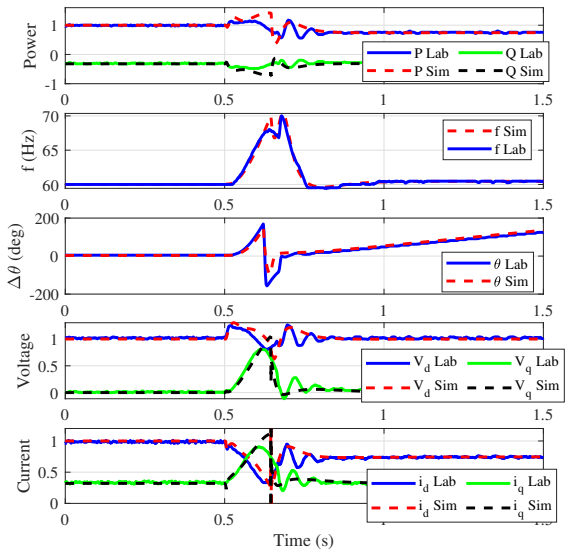


Fig. 14: Case B2: Event sequence.

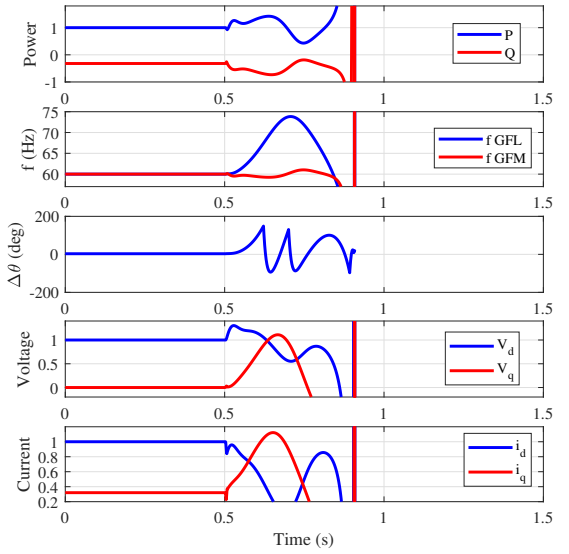
It can be seen that when the IBR sticks with the GFL control mode, a sudden islanding event breaks the system (shown in Fig. 15b. On the other hand, if we are able to switch the IBR from GFL to GFM in 6 cycles after the islanding event, the IBR can serve loads as a standalone microgrid Fig. 15a. The load in the islanding testbed is 0.75 pu. So after islanding, the IBR's power drops from 1 pu to 0.75 pu, and the frequency increases from 60 Hz to 60.45 Hz.

C. Category 3: Grid Fault Tests

In this section, three different kinds of grid disturbances



(a)



(b)

Fig. 15: Case B2: Hardware experiment results of a sudden islanding event at $t = 0.5$ s. (a) GFL to GFM switch occurs at about 0.6 s. (b) No control mode switching.

are presented and discussed. The first two cases focus on individual GFL or GFM's performance, while the last case demonstrates control mode switching upon a grid fault.

1) Case C1: Three-phase grid voltage magnitude dip: It is important to test the responses of an IBR towards grid disturbances. In this experiment (the event sequence is shown in Fig. 16), the responses of the VSC towards a balanced voltage dip when operating in either GFL or GFM control are compared side by side.

A balanced voltage magnitude dip is applied at the grid bus. Fig. 18 shows the instantaneous grid voltage measured using an oscilloscope. The voltage dip was triggered for 6 cycles from 1 to 0.3 pu. Fig. 17 shows the response of IBR

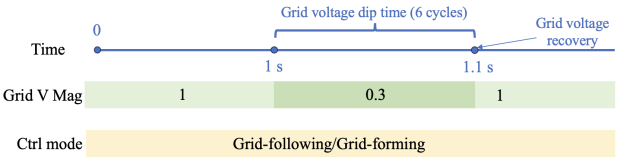


Fig. 16: Case C1: Event sequence.

in GFL or GFM for the grid voltage dip event. Both hardware experiment and the computer simulation results are presented. The results from the two environment show good agreement.

In the grid-following control, PLL is used for synchronization, which forces V_q to 0 at steady state. Upon a grid voltage dip, viewed from a synchronously rotating frame aligned with the PCC bus voltage space vector at steady state, V_d experiences a decrease while V_q experiences an increase immediately. This means that the PCC voltage vector experiences an immediate increase in angle. PLL's angle then follows this angle. Therefore the PLL frequency and angle will also increase. The detailed analysis can be found in [4].

Comparing Figs. 17a and 17b, we can see the clear difference between GFL and GFM. Particularly, the variations of frequency and angle of GFL are much greater than those of GFM. Indeed, large angle deviation has triggered 389 MW solar PV tripping in 2021 Texas Odessa event [3]. Analysis in [4] has shown that the PLL-based synchronization is the main contributor. In the GFM case, the synchronizing frame's angle increases upon voltage dip due to the reduction in real power measurement. Based on the experiment and simulation results, it can be seen that this frame almost aligns with the PCC voltage vector, leading to V_q maintaining 0 in the first 6 cycles.

Also notably, the dynamic response of real power of GFL is shown to have less variation compared to that of GFM. This is due to the constant real power control applied in the GFL. On the other hand, the GFM provides frequency support through real power variation.

The dynamic responses of reactive power Q and PCC bus voltage magnitude V_d are comparable for the GFL and GFM cases due to the same q-axis AC voltage control. The GFM's control is $3 + 40/s$ while the GFL's AC voltage control is $0.4 + 40/s$. This leads to slightly less variation in V_d for the GFM case.

2) Case C2: Weak grid tests: The weak grid tests have been conducted in computer simulation and the results are shown in Fig. 19a. The testbed was initially operated in GFL control mode before 2 seconds. At 1 second, there is a line tripping event changing the grid strength of the testbed from short circuit ration (SCR) at 3 to SCR at 1.5. Fig. 19a shows the system performed very well in the GFL mode when the grid strength is 3. However, when the line-tripping event happened, there are sustained 12.5 Hz oscillations observed from all measured components. After switching the control model to GFM at $t = 2$ s, the oscillations were damped-out within 0.4 seconds. This case shows the tolerance of weak grid condition regarding the GFM control is higher than GFL control. Thus, the switchable control design can be used to deal with weak grid condition if the system was initially operated

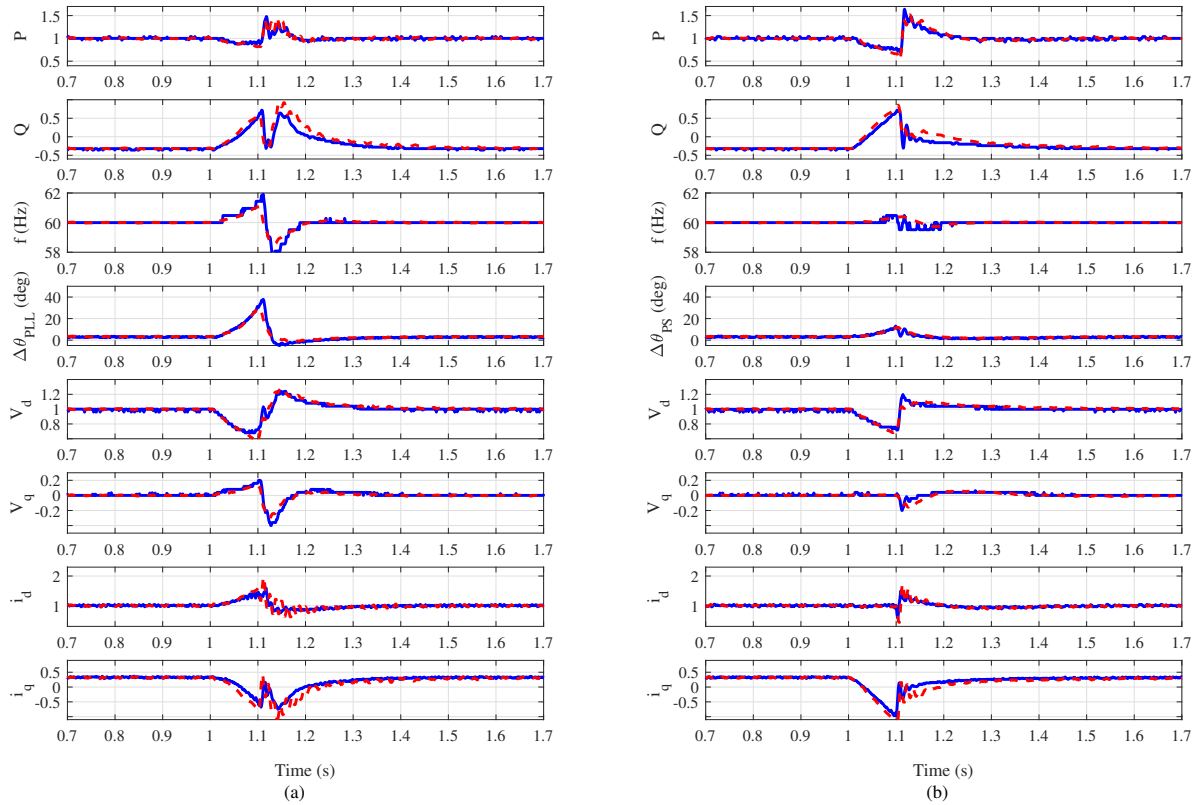


Fig. 17: Case C1: hardware experiment and computer simulation results of the grid voltage dip tests for GFL and GFM control. The blue line indicates the hardware result and the red dotted line indicate the simulation result. (a) GFL. (b) GFM.

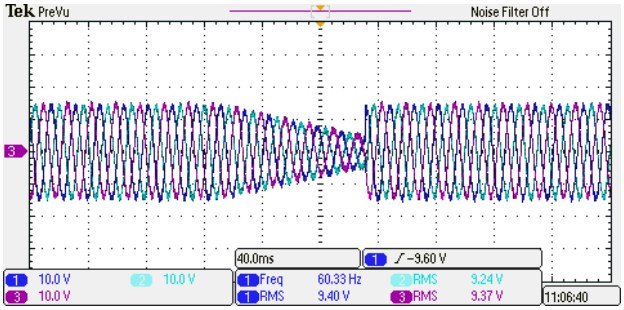


Fig. 18: Case C1: three-phase voltage drip applied to the grid voltage.

in GFL control mode. Fig. 19b shows the GFM control mode's boundary grid strength condition. The grid strength of the system changed from SCR = 0.95 to SCR = 0.8 at 1 second. It can be seen that the system loses synchronizing stability. The boundary condition result shows that the GFM can be operated under very low grid strength condition compared to a GFL, as remarked in [8].

3) Case C3: Line tripping and grid voltage dip: In this case, we demonstrate the benefit of control mode switching upon a grid fault. The grid fault occurs in a remote location. According to [31], a remote grid fault makes the equivalent Thévenin voltage viewed from the IBR drop. Therefore, an event timeline is designed and shown in Fig. 20. The grid strength measured by SCR and the grid voltage drop simultaneously at 0.5 seconds emulating a balanced 3-phase fault followed up by a line tripping event. The IBR switches from GFL to GFM after the fault with a delay of 6 cycles. The simulation results are shown in Fig. 21a. As a comparison, simulation results without control mode switching are also shown in Fig. 21b.

It can be seen that the system sticking with the GFL control goes unstable after the event, while the system comes back to steady state with the GFL to GFM control switch.

V. Conclusion

This paper presents the design and implementation of a switchable GFL and GFM control for a VSC in hardware. This control enables the VSC to operate in the grid-connected condition as a GFL controller or a GFM controller. When the VSC is operating in the islanded condition, it operates in the GFM control mode. The switchable GFL and GFM utilize the same sensors and has control logics designed to minimize transients during mode transients. The performance of the VSC has been tested in a hardware testbed. And the hardware experiment results show satisfactory performance, demonstrating the effectiveness of the VSC control design and the switching logics. In addition to offering the feasible and robust control design that has been successfully prototyped in hardware, this paper also contributes to in-depth dynamical analysis of GFL and GFM by associating responses observed in measurements with control logics. Particularly, this paper captures the subtle difference caused by different synchronization methods.

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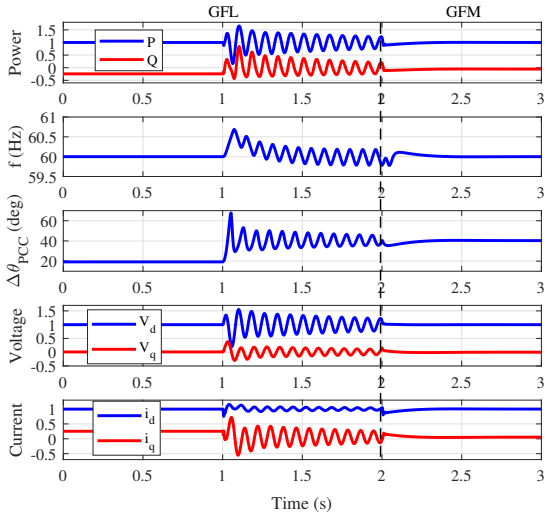
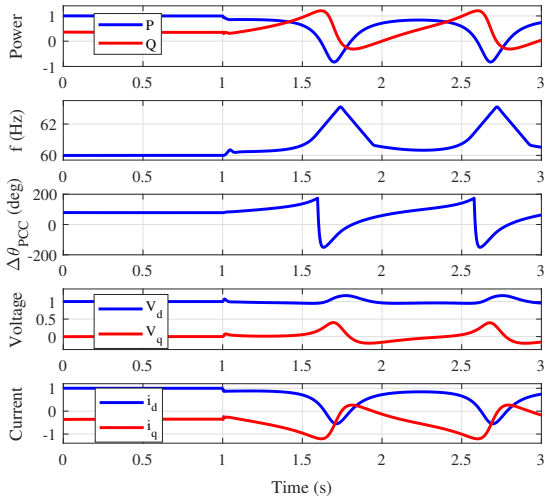


(a)



(b)

Fig. 19: Case C2: Weak grid condition tests. (a) Grid strength changes from SCR = 3 to SCR = 1.5 at $t = 1$ s, (b) GFM control. Grid strength changed from SCR = 0.95 to SCR = 0.85 at $t = 1$ s.

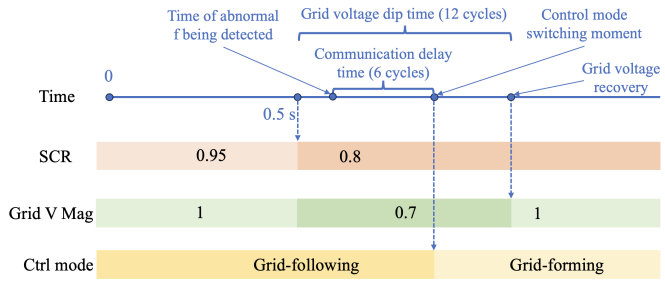
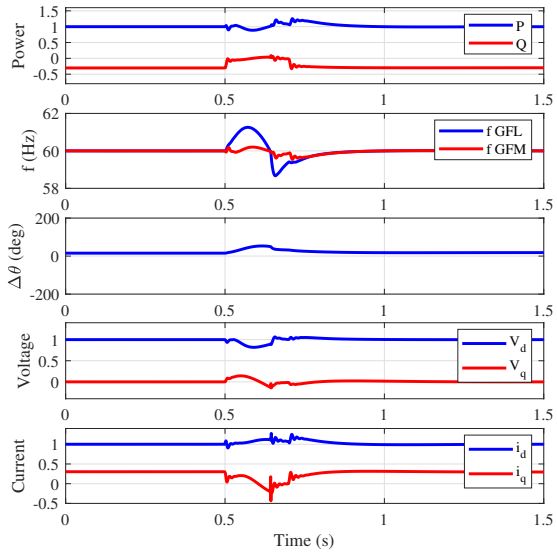


Fig. 20: Case C3: Event sequence of a grid voltage dip and line tripping case.



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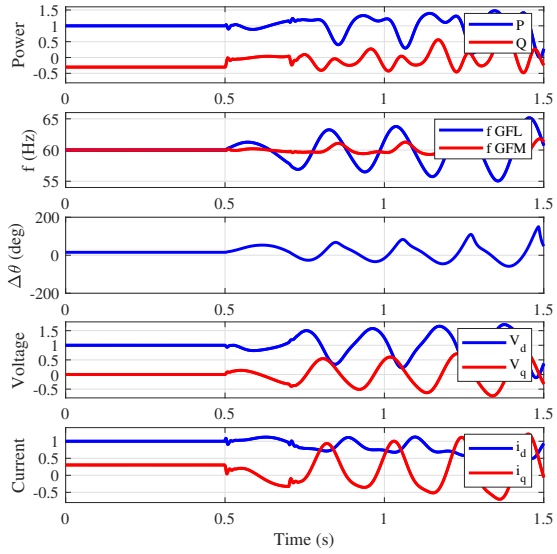

(b)

Fig. 21: Case C3: Computer simulation results for a grid voltage dip and line tripping event at $t = 0.5$ s. (a) GFL to GFM switching at 0.6 s; (b) no control mode switching.

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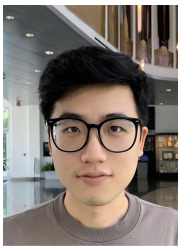

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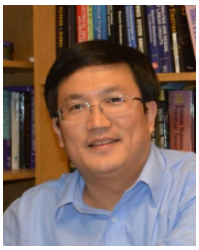

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