The Cause of Sub-Cycle Overvoltage: Capacitive Characteristics of Solar PVs

Lingling Fan, *Fellow, IEEE*, Zhixin Miao, *Senior Member, IEEE*

Abstract

In 2017 and 2018, large-scale solar photovoltaic (PV) tripping events occurred after transmission grid disturbances. Sub-cycle overvoltage is identified as the main cause that the PV inverters' protection systems initiated tripping actions. According to the reports from North American Electric Reliability Corporation (NERC), overvoltage is more severe at the PV inverter buses compared to the point of measurement (POM). Mechanism analysis of such a feature is an open research problem in the NERC community. This paper fills the gap. The goal of this paper is to explain why inverters may experience more severe overvoltage compared to the POM bus, which usually has shunt compensation installed. Through circuit construction with inverter control included, this paper will analyze and demonstrate the role of inverter control in aggravating overvoltage due to its capacitive nature in the subcycle dynamic range. While this nature is well known to the power electronics community, the current paper connects the dots to demonstrate how the capacitive nature of inverters can influence solar PV operation in a grid. A quantitative analysis is presented to explain the overvoltage mechanism.

Index Terms

Solar Photovoltaic (PV) grid integration; voltage source converter (VSC); sub-cycle overvoltage

I. Introduction

ON October 9 2017, 900 MW solar PVs tripped after transmission grid disturbances. The event is referred to as the Canyon 2 Fire event. According to the NERC report [1], sub-cycle overvoltage experienced at the solar PV inverter buses is the main cause of tripping. Following that event, in 2018, two more solar PV tripping events occurred in California, also due to sub-cycle overvoltage [2].

The NERC report [1] points out that inverter's momentary cessation, shunt compensation at the POM bus are interrelated to sub-cycle overvoltage. Plant operator(s) noted that many of the solar PV plants affected by the disturbance have shunt capacitor banks within the plant. In addition, overvoltage is much more severe at the solar PV inverter bus compared to that at the POM. This issue was singled out as a key finding and further study to develop a better understanding was recommended by NERC.

In the authors' prior research [3], sub-cycle overvoltage in a shunt compensated network with solar PVs' momentary cessation acting as the trigger is demonstrated. Analysis in [3] shows that shunt compensation is critical to create an LC mode of more than 150 Hz. This mode may be triggered by sudden inverter current ramp down, or momentary cessation, leading to overvoltage most severe at the capacitor bus. In [3], the shunt compensation is assumed to be connected at the inverter bus. Therefore, the inverter bus shows the most severe overvoltage. On the other hand, this assumption of the network topology deviates from the real-world circuit topologies. Shunt capacitors are usually installed at a substation bus, or the POM. Between a solar PV and the substation, there exist collecting lines and step-up transformers to boost the output voltage of a PV plant.

If the sub-cycle overvoltage is predominantly caused by the interaction of the shunt capacitor and the grid inductive impedance, overvoltage would be most severe at the substation bus. This is not the case observed in real world. Therefore, it is reasonable to speculate that solar PV's own characteristic plays a role in sub-cycle overvoltage aggravation. The focus of this research is on examining PV inverter's current control that leads to a capacitive characteristics. It is true that solar PV's

This project is supported in part by US Department of Energy DE-EE-0008771. L. Fan and Z. Miao are with University of South Florida, Tampa FL, 33620. e-mail: {linglingfan, zmiao}@usf.edu.

terminal LCL filters may also contribute to the capacitive characteristics. On the other hand, the size of a shunt capacitor of a filter is usually very small. Contribution to overvoltage is very limited. Hence, the impact of a filter is ignored.

This paper offers a quantitative analysis to explain the role of inverter control in aggravating sub-cycle overvoltage. This paper will set to analyze the frequency responses of inverter controls. Furthermore, through circuit construction with inverter control included, the frequency-domain responses of two transfer functions (the PCC voltage vs. the inverter current order, and the POM voltage vs. the inverter current order) can be found. It can be clearly shown that the first transfer function has a larger magnitude compared to the second one. Thus, the inverter bus is expected to experience more severe overvoltage. Time-domain simulation results based on the circuit further demonstrate the overvoltage and provide sensitivity analysis regarding inverter control and shunt compensation.

The contribution of our paper is the plausible mechanism analysis of sub-cycle overvoltage observed in real-world events. This mechanism analysis is an open research problem in the NERC community and it has not been tackled by other researchers. Our paper fills the gap.

In the remainder of the paper, section II presents the test bed information and the circuit representation in the frequency domain. Section III provides analysis and simulation results. Section IV concludes the paper.

II. Circuit Representation

The circuit topology is shown in Fig. 1. A solar PV is connected to its point of common coupling (PCC) bus through a choke filter, with a reactance of 0.15 p.u.. This circuit is expressed in per unit system, where $R_X + sL_X$ represents the aggregated transformer and collecting line impedance, sC represents the admittance of the shunt capacitor. The grid is viewed at the substation or POM as a constant voltage source v_g behind an impedance $R_g + sL_g$. R/X ratio of the system is assumed as 10%. The shunt compensation is assumed to be 30% of the solar PV's rated power and the source impedance is assumed to have a reactance of 0.15 p.u.. The transformer reactance is 0.30 p.u.. 30% shunt compensation is in the typical range of solar PV shunt compensation. The aggregated impedance of the transformer and the collection line is chosen based on typical values. A solar PV requires a step up transformer to boost voltage to mid-level (e.g., 13.2 kV) and another transformer to boost to the bulk system level (e.g., 161 kV). Each transformer has a 0.1 p.u. reactance. The reactance of the collection line is assumed as 0.1 p.u.. Thus, the aggregated reactance of L_X is 0.3 p.u..

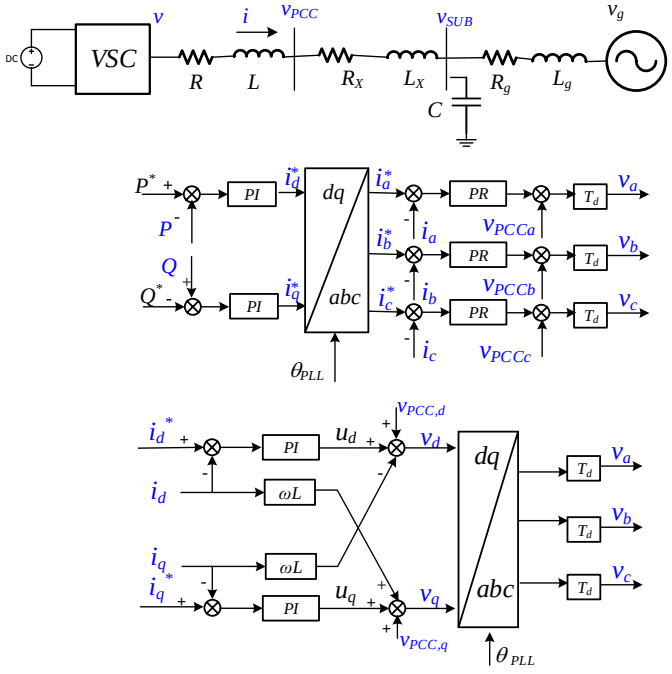


Fig. 1: The circuit topology and the assumed VSC control structure. Proportional and resonant gains of the PR controller: 0.25, 10. Proportional and integral gains of the PI controller: 0.25, 125. Delay: 100 μs.

The PV system's impedance will be derived based on the typical converter controls. Since the focus is on sub-cycle dynamics at about $150-250$ Hz, the converter's slow outer-loop controls and phase-lock-loop (PLL) are not considered, while the effect of fast inner current controls and delay due to pulse width modulation and communication is considered and notated as $T_d(s) = e^{-s\tau}$, where τ is the delay time and $100\,\mu$s is a typical number.

Two types of inner converter control structures are commonly used: proportional resonant (PR) control based on stationary frame, and proportional integral (PI) control based on a dq frame. For both current control structures, the PCC voltage feedforward unit is included. The overall control structures are shown in Fig. 1. The transfer functions of the PR control viewed from the abc frame (notated as $H_{\rm PR}(s)$), the PI control viewed from the dq frame (notated as $H_{\rm PI}(s)$), and the PI control viewed from the abc frame (notated as $H^s_{\rm PI}(s)$) are:

$$H_{\rm PR}(s) = K_p + K_r \frac{2\omega_c s}{s^2 + 2\omega_c s + \omega^2}. \tag{1}$$

$$H_{\rm PI}(s) = K_p + \frac{K_i}{s},\ \ H^s_{\rm PI}(s) = K_p + \frac{K_i}{s - j\omega} \tag{2}$$

where ω is the nominal frequency at 377 rad/s and ω_c is $2\pi \times 2$ rad/s.

The system will be viewed from the PCC bus as two components: the solar PV $Z_{\rm pv}$ and the grid $Z_{\rm grid}$. The grid impedance consists of the transformer, the shunt capacitor, and the source impedance: $Z_{\rm grid}(s) = R_{\rm x} + sL_{\rm x} + \frac{1}{sC + \frac{1}{R_g + sL_g}}$. Its magnitude has a peak at the frequency of $\frac{1}{\sqrt{L_g C}}$ (283 Hz) followed by a dip at the frequency of $\frac{L_X + L_g}{L_X L_g C}$ (346 Hz).

The solar PV's impedance will be derived. Based on the circuit, the converter's output voltage v, output current i, and the PCC voltage $v_{\rm PCC}$ can be expressed by (3). Based on the control logic, the three variables are expressed by (4) or (5).

$$v = v_{\rm PCC} + (R + sL)i \tag{3}$$

$$\text{PR: } v = \left(v_{\rm PCC} + H_{\rm PR}(s)(i^* - i)\right) T_d(s) \tag{4}$$

$$\text{PI: } v = \left(v_{\rm PCC} + H^s_{\rm PI}(s)(i^* - i) + j\omega L i\right) T_d(s) \tag{5}$$

Based on (3), (4), and (5), the PV can be represented as a Thevenin equivalent circuit viewed from the PCC bus:

$$v_{\rm PCC} = \underbrace{\left(\frac{T_d}{1 - T_d} H_{\rm PR}(s)\right)}_{Z^*_{\rm PV}} i^* - \underbrace{\left(\frac{T_d H_{\rm PR}(s) + R + sL)}{1 - T_d}\right)}_{Z_{\rm PV}} i \tag{6}$$

$$v_{\rm PCC} = \underbrace{\left(\frac{T_d}{1 - T_d} H^s_{\rm PI}(s)\right)}_{Z^*_{\rm PV}} i^* - \underbrace{\left(\frac{T_d(H^s_{\rm PI}(s) - j\omega L) + R + sL}{1 - T_d}\right)}_{Z_{\rm PV}} i. \tag{7}$$

Its Norton equivalent can also be found as

$$i = Y_{\rm PV} Z^*_{\rm PV} \cdot i^* - Y_{\rm PV} \cdot v_{\rm PCC}, \tag{8}$$

where $Y_{\rm PV} = 1/Z_{\rm PV}$.

Circuit analysis leads to the expressions of the PCC voltage and the substation voltage in terms of the grid voltage v_g and the converter current order i^*.

$$v_{\rm PCC} = (Y_{\rm PV} + Y_{\rm grid})^{-1} \left(Y_{\rm PV} Z^*_{\rm PV} i^* + \frac{v_g}{(sCZ_g + 1)Z_{\rm grid}}\right) \tag{9}$$

$$v_{\rm SUB} = \left(\frac{1}{Z_{\rm PV} + Z_X} + sC + y_g\right)^{-1} \left(\frac{Z^*_{\rm PV}}{Z_{\rm PV} + Z_X} i^* + y_g v_g\right) \tag{10}$$

III. Analysis and Simulation Results

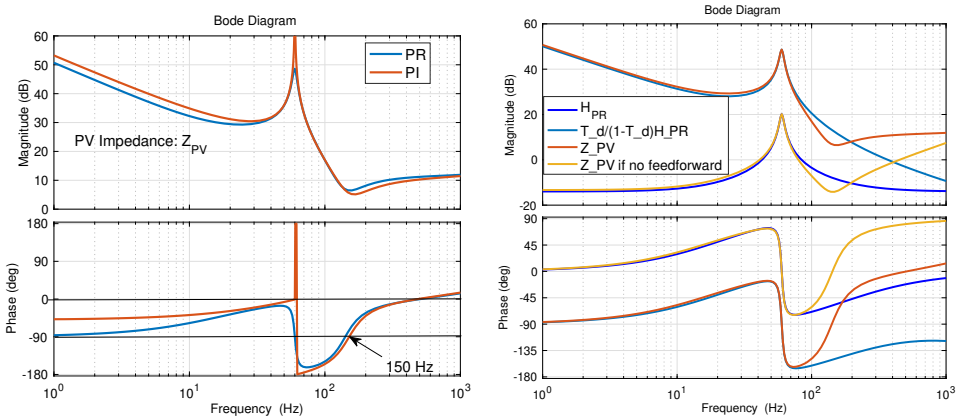
A. Sensitivity analysis of inverter control

The PR control and PI control parameters are selected to have the control controller's bandwidth at 225 Hz in the abc frame. The parameters are shown in the caption of Fig. 1. Fig. 2a presents the Bode plots of the PV impedance $Z_{\rm PV}$ for two types of controls, expressed in (6) and (7). It can be seen that the PV impedance is capacitive below 400 Hz. In addition, from 60 Hz to 150 Hz, PV impedance is not only capacitive but also with a negative resistance. Particularly, at 150 Hz, the PV's impedance with PR control is $-j2.5$ p.u., equivalent to a shunt capacitor of the size of 0.4 p.u. The size of the equivalent shunt compensation is comparable to the size of the shunt compensation located at the POM or substation (0.3 p.u.). Thus, it is expected that the inverter's PCC bus will experience more several overvoltage compared to the substation bus.

It can also be seen that both control structures lead to the same impedance responses in the supersynchronous frequency range. Hereafter, we will focus on the PR control only.

Fig. 2b further presents the frequency responses of the PR control, the PR control along with delay and feedforward, the PV impedance with the effect of the feedforward and delay, and the PV impedance if there is no feedforward. If there is no delay, the PV inverter is a current source only. If there is no feedforward, the PV inverter's impedance is $T_d H_{\rm PR}(s) + R + Ls$. It can be seen that while the introduction of feedforward unit significantly increases the impedance magnitude, making an inverter less susceptible to external voltage disturbances, the feedforward unit and the delay also introduce negative resistance and capacitance into the impedance.

Remarks: Delay and feedforward introduce negative resistance and capacitive feature in the frequency range of 60 Hz- 150 Hz.



(a) (b)

Fig. 2: (2a) PV impedance for two types of current controls. (2b) $H_{\rm PR}$, $\frac{T_d}{1-T_d}H_{\rm PR}$, $Z_{\rm PV}$, and $Z_{\rm PV}$ if there is no feedforward unit.

B. Admittance and impedance

The total admittance viewed at the PCC bus ($Y_{\rm PV} + Y_{\rm grid}$) is shown in Fig. 3a. It can be seen that the grid admittance has a dip at 283 Hz and a peak at 346 Hz, due to the LCL circuit characteristic. Combining the PV and the grid admittances leads to the total admittance, which has a dip at ~ 150 Hz. This dip is due to the capacitive component of the PV admittance canceling the inductive component of the grid admittance.

The dip in the total admittance results in a peak in the total impedance viewed from the PCC bus, in turn, a peak in the transfer functions from the current order to the PCC and substation voltages, as shown in Fig. 3b. It is to be noted that an obvious difference in the peak gain of the two transfer functions. The PCC voltage versus the current order shows a peak gain of 11.8 dB while the substation voltage versus the current order shows peak gain of 4 dB at 150 Hz. Therefore, it is expected to see more severe overvoltage in the PCC bus, compared to the substation bus. The two peak gains indicate that the change in the PCC voltage is expected to be 2.45 times of that in the POM voltage, upon an inverter current order change.

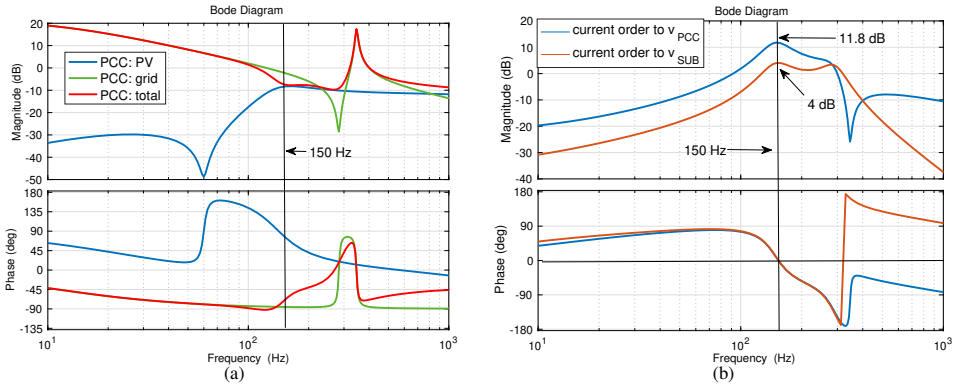


Fig. 3: (a) Admittances viewed at the PCC bus: PV admittance, grid admittance, and the total admittance. (b) Two transfer functions: from the current order to the PCC voltage and from the current order to the substation voltage.

C. Time-domain simulation results

The time-domain simulation results based on the linear system are presented in Fig. 4. All three voltages, the grid, the substation, and the PCC are initially working at 1 p.u.. At 0.18 s, the grid voltage has a 10% dip in its magnitude. At 0.20 s, the current order ramps down from 1.12 to 0. It can be seen that the PCC voltage experiences 1.53 p.u. overvoltage in 0.004 s or a quarter cycle. On the other hand, the substation voltage has a maximum of 1.18 p.u..

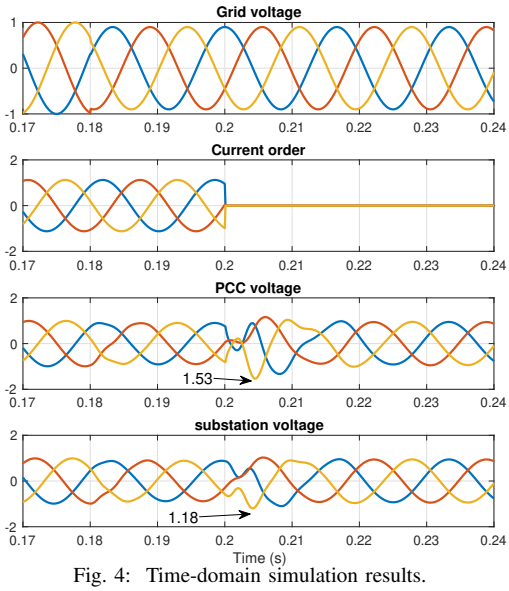


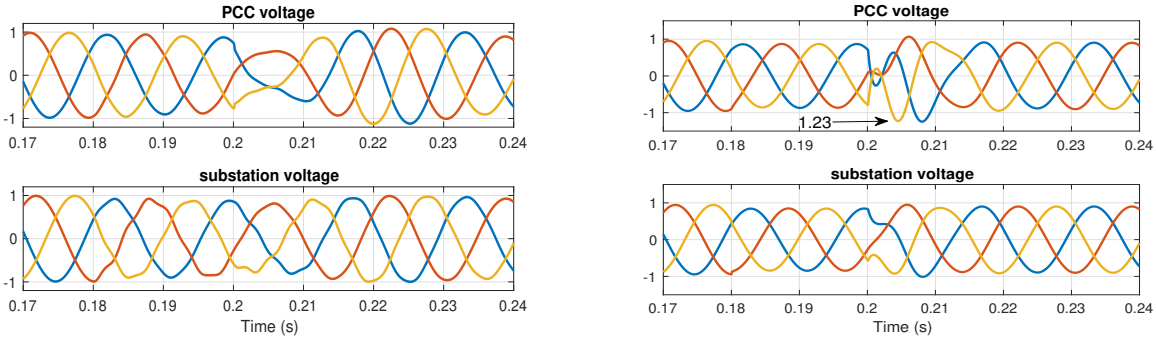
Fig. 4: Time-domain simulation results.

Sensitivity Analysis: Effect of the feedforward and the shunt capacitor is also examined. Without the feedforward unit, the PV impedance is much smaller, about 10% of the one with feedforward at 100 Hz range, as shown in Fig. 2(b). This effect makes the PV admittance much larger and the contribution from the current order to the PCC voltage is much smaller. Fig. 5a and Fig. 5b present the simulation results. It can be seen that ramping down current order does not cause any overvoltage if the feedforward unit is not employed. It can also be seen that overvoltage is much less severe if there is no shunt compensation.

Remarks: The analysis and simulation results confirm the remarks of the NERC report: interaction of solar PVs, shunt compensation, and momentary cessation leads to overvoltage. Furthermore, the analysis also addresses why overvoltage is more severe at the inverter bus than that at the POM. In short, the inverter's own capacitive and negative resistive nature in the subcycle time scale contributes to overvotage.

IV. Conclusions

This short communication provides a quantitative analysis on why sub-cycle overvoltage is more severe at the solar PV inverter bus than that at the POM bus. It is found that solar PV's capacitive characteristic contributes to overvoltage. The



(a) (b)

Fig. 5: Simulation results. (a) Without feedforward unit. (b) Without shunt compensation.

feedforward unit used in converter current control and the shunt compensation all exacerbate overvolage.

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