High-Frequency Oscillations in Grid-Connected Voltage-Sourced Converters

Huazhao Ding, Lingling Fan, Zhixin Miao
Department of Electrical Engineering
University of South Florida
Tampa, FL 33620, USA
email: {huazhao, linglingfan, zmiao}@usf.edu

***Abstract*—This paper investigates high-frequency oscillations (HFOs) in a three-phase grid-connected voltage-sourced converter (VSC). The main work is modeling and mechanism analysis of HFO above 1000 Hz. An electromagnetic transient (EMT) test bed including 5 kHz power electronics switching sequences is set up for conducting simulation experiments. Furthermore, impedance-based analytical model is developed for linear analysis. It is found that both control delay and LCL filter play roles in HFO generation. The analysis results collaborate the simulation results from the EMT test bed.**

***Index Terms*—Three-phase VSC, high-frequency oscillations, delay.**

I. Introduction

HIGH frequency oscillation (HFO) events have been reported in recent years around the world [1]–[4]. In south China, HFOs at 1272 Hz have been observed in a modular multilevel converter (MMC)-based high voltage direct current (HVdc) system located in Luxi [1], [2]. In Europe, offshore wind power plants (WPP) have also observed HFOs in the frequency range of a few hundred Hz to 800 Hz [3], [4].

For the Luxi event, [1], [2], [5], [6] provide analysis. [2] found HVdc converter's outer control loops and PLL have negligible impact due to their slow control bandwidth. Therefore, [5] focuses on analyzing converter's current control and grid interactions. [5] found that the low-pass filter (LPF) applied on the PI current control and PCC feedforward voltage has less influence on the high-frequency instability, while the reactance of the filter between the VSC output side and PCC bus will influence the HFO more significantly. Furthermore, [6] implemented a pure reactance filter in the system to replicate the HFO in the Luxi project and developed an adaptive notch filter applied on the controller side to eliminate the HFO.

For WPP HFOs, analysis and mitigation have been conducted in [7]–[10]. It is found from these papers that LCL filter and control delay can result in HFOs [7], [8]. Specifically, control delay's effect in introducing negative resistance or damping is pointed out in [9]. In [10], Larsen and Sun indicate that the offshore wind energy delivery system has it circuit components designed with small resistance to reduce power loss. This design makes HFOs have insufficient damping. [10] provides a mitigation solution: installing analog filters at the WPP substation to provide damping of HFOs.

This work is supported in part by DOE SETO award DE-EE-0008771.

The goal of this paper is to set up a simple EMT test bed consisting of a single VSC to demonstrate HFO phenomena and further conduct analysis to examine the influence factors of HFO. This paper examines the test bed topologies in the literature [5], [7], [8], and designs a test bed topology that can successfully demonstrate HFO. Furthermore, analysis is provided to identify the critical influencing factors on HFO: control delay and LCL filter.

It has to be mentioned that the test beds in [5] do not include LCL filter while [8] includes LCL filter. To demonstrate HFO, in our first attempt, the hardware test bed in [5] is replicated in EMT simulation environment (MATLAB/Simscape). For this set up, the grid impedance is represented by the cable model used in [5]. Further tuning of the test bed includes to install an LCL filter. With this set up, HFOs can be demonstrated when control delay is increased.

Other uniqueness of this paper is the investigation is based on stationary frame current control This is different from the literature [5], [7], [8] and can provide another perspective of HFO, i.e., HFO can appear whether the current control is implemented in a dq frame or a stationary frame.

The rest of the paper is organized as follows. Section II introduces the structure of the system and control topology. Section III presents the EMT simulation results that demonstrate HFO. Section IV presents the derivation of the analytical model and the analysis of HFO. Furthermore, comparison of the results based on the analytical model and the EMT test bed is discussed. Section V concludes the paper.

II. Structure of the test bed and VSC control

The topology of a grid-connected three-phase VSC is shown as Fig. 1. A three-phase VSC is connected to the infinite bus v_g through an LCL-filter and a cable. The left side of the LCL filter is the VSC output bus notated as v_o, while the right side of the LCL filter is the point of common coupling (PCC) bus notated as $v_{\rm PCC}$. The cable connects the PCC bus and infinite bus. Each phase of the cable is represented by two parallel-connected branches. One is a serial connected resistor and capacitor, the other one is an inductor. The whole system has two sources connected. One is a 200-V DC voltage source connected to the VSC and the other one is an 80-V AC voltage source that served as the grid.

978-1-6654-9921-7/22/$31.00 ©2022 IEEE

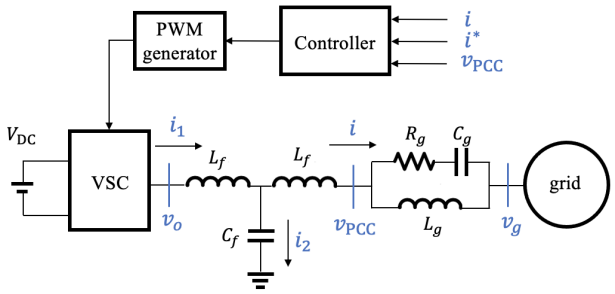

Fig. 1: Structure of the system.

The parameters related to the testbed and the LCL-filter are based on [5] and [7], respectively. Analysis in this paper is carried out via per unit value. The SI values and the per unit (pu) values corresponding to all parameters are listed in Table I.

TABLE I: Main parameters of the system

Description	Item	Value	Per unit
Rated Power	S_{base}	1×10^3 W	1 pu
Rated Voltage	V_{base}	80 V	1 pu
LCL-filter inductor	L_f	8×10^{-4} Ω	1.25×10^{-4} pu
LCL-filter capacitor	C_f	15×10^{-6} F	9.6×10^{-5} pu
Cable resistor	R_g	6 Ω	0.9375 pu
Cable inductor	L_g	8×10^{-3} H	2.5×10^{-3} pu
Cable capacitor	C_g	9×10^{-6} F	5.76×10^{-5} pu
Nominal Frequency	f	50 Hz	1 pu

A. VSC control topology

The converter is assumed to have a current control implemented in the stationary frame. Thus, it requires the each phase current to track an order. This current order is a sinusoidal signal. To track sinusoidal signals, proportional resonant (PR) control is a popular method. In this VSC control, the PR current control along with the PCC voltage feedforward unit generates the converter voltage references for the pulse width modulation (PWM). In addition, a first-order low pass filter (LPF) is applied on the feedforward PCC voltage to filter out high-frequency noise and make the whole system more stable. The structure of the VSC control is shown in Fig. 2.

The transfer functions of the PR controller and the first-order LPF are expressed as follows.

$$G_{\text{PR}}(s) = k_p + \frac{k_r \cdot 2\omega_c \cdot s}{s^2 + 2\omega_c \cdot s + w_0^2}, \tag{1}$$

$$G_{\text{LPF}}(s) = \frac{1}{1 + \tau_1 \cdot s}, \tag{2}$$

where s is the Laplace operator, the cutoff frequency ω_c is 4π rad/s, ω_0 is 377 rad/s, time constant τ_1 in LPF is assumed as 0.001 s. The PR gains are set as (k_p, k_r) = (0.8, 69).

The control delay $T_d(s)$ is implemented between the VSC control output and the references to the PWM generator. $T_d(s)$ represents the delay caused by the communication of the inner current controller and the delay caused by the PWM. For the EMT test bed, the carrier frequency of the PWM is 5000 Hz.

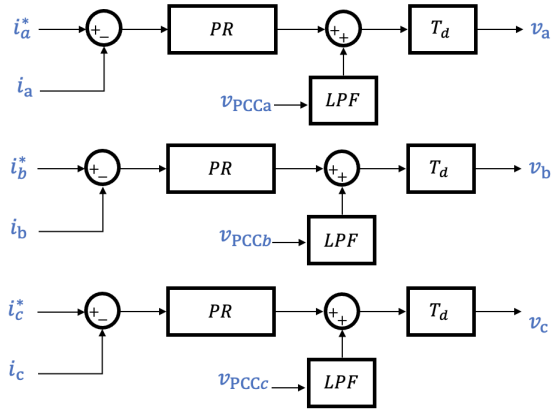

Fig. 2: Block diagram of the VSC control.

III. EMT TESTBED SIMULATION RESULTS

To study the system, the test bed with PR current control is built as Fig. 1 and Fig. 2 in MATLAB/SimScape. The control delay is represented by the transport delay block, which is put right behind the control topology.

The objective of this paper is to analyze HFOs. HFOs will be triggered by changing the delay time constant. The control delay time constant is initially given as 100 μs. After $t = 1$ s, the delay becomes 180 μs.

Fig. 3 presents the measured phase A current from the PCC bus. Before 1 s, as the reference current is given as 0.5 pu, phase A current is at 0.5 pu without much harmonics and oscillations. After 1 s, the phase A current is distorted. It is easy to observe that the system is suffering harmonic instability.

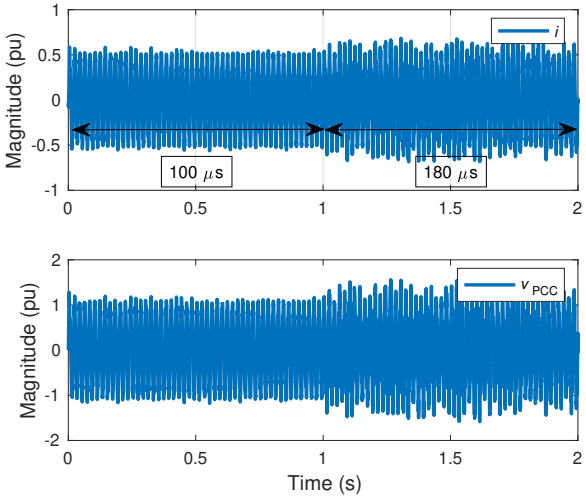

Fig. 3: Phase A PCC reference current and measured current.

Fast Fourier transform (FFT) analysis is applied to analyze the frequency spectrum distribution in phase A PCC current for both the stable condition and the harmonic condition. The range that adopted to do the FFT analysis are from 0.2 s to

0.4 s and from 1.2 s to 1.4 s. The spectrum at both 100 μs delay time and 180 μs delay time are shown in Fig. 4.

In Fig. 4, the red curve shows the frequency distribution when the control delay is 100 μs, while the blue curve shows the frequency distribution when the delay time is 180 μs.

Before 1 s, a 179-Hz component with less than 0.5% magnitude could be observed. For the high-frequency region, especially after 1000 Hz, harmonics could be observed but have very small magnitudes.

After 1 s, when the delay time equals 180 μs, a 1340-Hz component becomes dominant (3.5% pu magnitude) besides the 60-Hz fundamental component. Compared these two cases, it can be seen that control delay increase in this range does not influence the low-frequency region but has a significant impact on the high frequency region at about 1300 Hz.

For a delay $e^{-\tau s}$ to introduce -90° phase angle, the frequency is

$$\frac{\frac{\pi}{2}}{\tau} \text{ rad/s} = \frac{1}{4\tau} \text{ Hz}.$$

Thus, if τ is 100 μs, this frequency is 2500 Hz. If τ is 180 μs, this frequency is 1389 Hz.

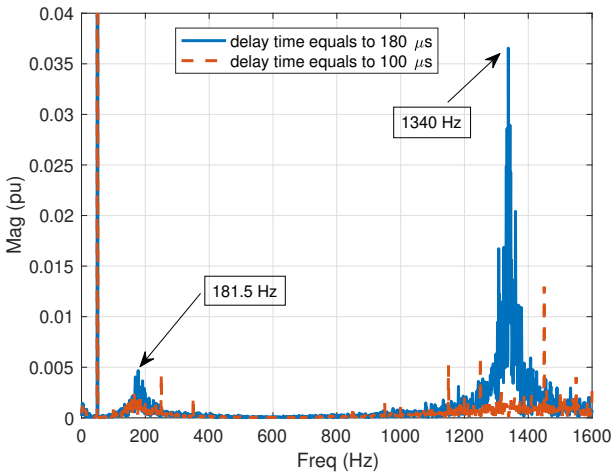

Fig. 4: FFT analysis of phase A PCC current before 1 second and after 1 second.

IV. Analysis

For analysis, the impedance models are derived and their frequency responses are compared. Thus, the whole system is viewed at the PCC bus as two subsystems: the VSC and the grid. The first subsystem VSC includes the LCL filter and the VSC control. The equivalent impedance of this part is regarded as $Z_c(s)$. The second subsystem is viewed from the PCC bus to the grid. The equivalent impedance is regarded as $Z_g(s)$.

The grid impedance is notated as $Z_g(s)$ and it is derived based on the cable model with two parallel branches.

$$Z_g(s) = \frac{(R_g + \frac{1}{sC_g}) \cdot sL_g}{R_g + \frac{1}{sC_g} + sL_g}. \tag{3}$$

The impedance of the VSC cannot be acquired directly. This impedance reflects the relationship between the PCC voltage $v_{\text{PCC}}$and the current flowing out of the LCL filter i. It will be derived using both the control logic and the circuit relationship, both associated with the VSC output voltage v_o and the VSC output current i_1.

A. Circuit

For circuit relationship, the VSC output voltage v_o and the PCC bus voltage v_{PCC} are associated with the two currents i_1 and iL

$$v_o = v_{\text{PCC}} + sL_f \cdot i + sL_f \cdot i_1. \tag{4}$$

Assume that current through the shunt C_f is i_2. This current is related to the converter current i_1 and the LCL filter current i as follows:

$$i_2 = i_1 - i. \tag{5}$$

Thus, the VSC output current i_1 could be expressed as (6):

$$i_1 = i + \underbrace{sC_f \cdot (v_{\text{PCC}} + sL_f \cdot i)}_{i_2}. \tag{6}$$

With (6) and Eq. (4), the VSC output voltage v_o can be expressed by the PCC voltage v_{PCC} and the output current i only:

$$v_o = v_{\text{PCC}} + 2sL_f \cdot i + s^3 L_f^2 C_f \cdot i + s^2 L_f C_f \cdot v_{\text{PCC}}. \tag{7}$$

B. Control logic

v_o can also be expressed by the PCC voltage v_{PCC} and the output current i through the control logic.

The principle of the VSC control is shown in Fig. 2. For the control delay $T_d = e^{-\tau s}$, it is approximated by using the Pade expression as shown in (8).

$$T_d(s) = e^{-\tau s} \approx \frac{1 - s \cdot \tau/2}{1 + s \cdot \tau/2} \tag{8}$$

With the expression of the control delay, the VSC output voltage from the PR current controller side could be derived as (9), where i^* is the PCC reference current.

$$v_o = G_{\text{LPF}} T_d v_{\text{PCC}} + G_{\text{PR}} T_d (i^* - i) \tag{9}$$

Combining (7) and (9) leads to the cancelation of the VSC output voltage v_o. The relationship between PCC voltage v_{PCC}, the current reference i^* and the measured current i is shown in (10).

Eq. (10) indicates that viewed from the PCC bus, the VSC is a Thevenin equivalent with a voltage source v_c behind an impedance Z_c. Based on (3) and (10), the simplified structure of the testbed could be derived with a voltage source v_c connected to grid through controller side impedance Z_c and grid side impedance Z_g. The simplified structure is shown as Fig. 5 Thus, the stability of the system could be analyzed by comparing grid side impedance and controller side impedance.

$$v_{\mathrm{PCC}} = \underbrace{\left(\frac{G_{\mathrm{PR}}(s)\cdot T_d(s)}{1+s^2L_f\cdot C_f - G_{\mathrm{LPF}}(s)\cdot T_d(s)}\right)}_{V_c} i^* - \underbrace{\left(\frac{G_{\mathrm{PR}}(s)\cdot T_d(s) + 2sL_f + s^3L_f^2\cdot C_f}{1+s^2L_f\cdot C_f - G_{\mathrm{LPF}}(s)\cdot T_d(s)}\right)}_{Z_c(s)} i \tag{10}$$

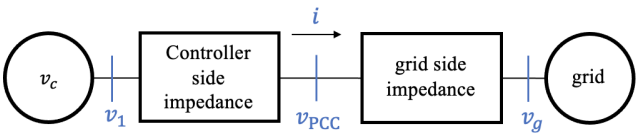

Fig. 5: The simplified structure of the system.

C. Control delay analysis

Based on (3) and (10), the grid side impedance Z_g and controller side impedance Z_c are plotted in Fig. 6 for stability analysis.

Z_c under two control delay time constants are presented. It can be seen that increasing the delay time constant changes both the magnitudes and phase angle of Z_c in the range of 400 Hz to 2000 Hz.

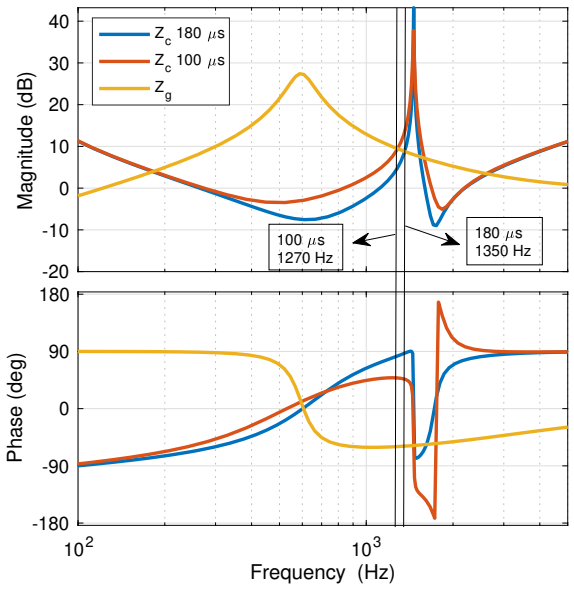

Fig. 6: VSC impedance and grid impedance viewed at PCC bus.

In Fig. 6, the blue line represents the controller side impedance Z_c when the control delay time is 180 μs. Z_c and Z_g have the same magnitude at four crossover points, which means the open-loop transfer function $Z_c(s)/Z_g(s)$ is 1 at those crossover frequencies.

The first two crossover frequencies are 182 Hz and 1350 Hz, respectively. Also, there have another two cross points. The other two are 1600 Hz and 2640 Hz. For the first two points, the phase difference between grid impedance Z_g and controller side impedance Z_c are all close to 180 degrees. This means that the two harmonic components at those frequencies may be visible in measurements.

For the last two crossover points, the phase angle between cable impedance and controller side impedance is much less than 180 degrees, indicating that the system should be stable at these two crossover frequencies.

The above analysis successfully explains why the FFT analysis of the current measurements from the EMT test bed show both 180-Hz and 1350-Hz components. Thus, when the delay time is 180 μs, the analytical model could find the HFO at 1350 Hz.

For comparison, Fig. 6 also shows Z_c when the delay time is 100 μs in red line. It is obvious to find that the magnitudes of Z_g and Z_c also meet 182 Hz with a phase angle difference closing to 180 degree. This implicates that decrease control delay time will not influence the low frequency dynamics. However, the frequency of the second crossing point reduces from 1350 Hz to 1270 Hz. Moreover, the phase angle between of Z_c and Z_g at 1270 Hz is much less than 180 degree, implicating an insignificant harmonics at 1270 Hz.

Remark: The analysis provided clearly shows that influence of control delay's impact in changing dynamics of the system at 1000 Hz frequency range. Increasing control delay can make HFO appear.

D. Negative damping

Reference [9] has explicitly pointed out that control delay introduces negative damping at certain frequency range. To validate and demonstrate this point, the real and imaginary parts of Z_c under two delay time constants are plotted in Fig. 7.

In Fig. 7, the blue line shows the real part of Z_c, when the control delay time equals 180 μs. It is obvious that the resistance has a magnitude dip to 0 at 1420 Hz. For 100 μs delay time, the resistance is much large in the frequency range of 1000 -1400 Hz. This indicates that adding control delay time will cause negative damping in this frequency range for this particular VSC.

E. LCL-filter sensitivity analysis

From (10), it can be seen Z_c has a pair of poles influenced by L_f and C_f. Increasing L_f or C_f will reduce the frequency of the poles. The poles are reflected as the peak in Z_c's magnitude in its Bode plots.

To perform the sensitivity analysis of LCL-filter, double sized filter inductor and capacitor of controller side impedance are examined in Fig. 8. It can be seen that increasing the size of L_f and C_f can make HFO have lower frequency.

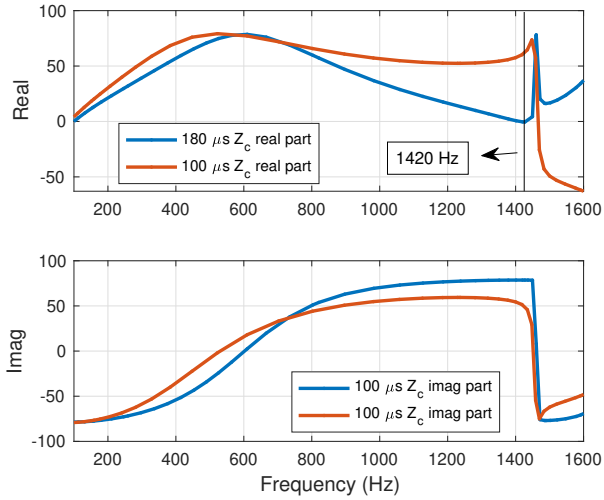

Fig. 7: Real and imaginary parts of Z_c.

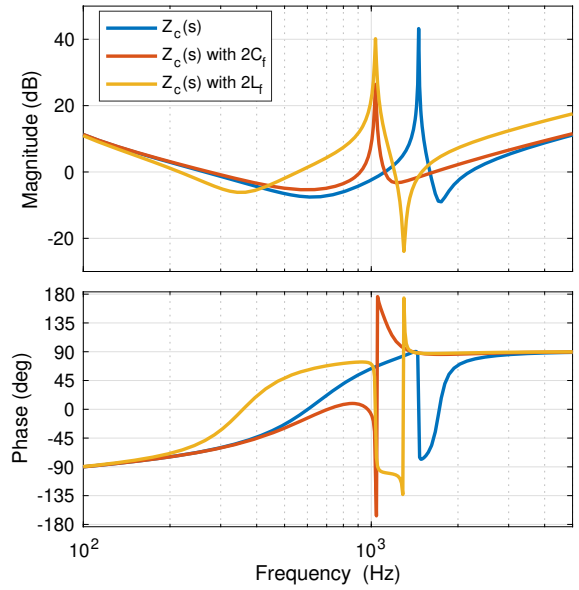

Fig. 8: Sensitivity analysis of the LCL-filter.

Simulation results of the analytical model and EMT model are documented in Table. II.

TABLE II: Simulation result of analytical model, Root Locus model and EMT model.

Model	**Low frequency** (Hz)	**High frequency** (Hz)
Impedance-based	182	1350
EMT	181.5	1340

In Table. II, low-frequency oscillations for these two models are around 181 Hz, while the HFOs are all around 1350 Hz. The difference between the analytical model and the EMT model is calculated, which is within 3 percent. Due to the tiny difference between the EMT model and the analytical model, these two simulation results could be regarded as matched. This confirms that adding delay time will result in HFO issues.

V. Conclusion

In this paper, a three-phase VSC system with LCL-filter and cable is modeled and simulated to analyze the HFO caused by control delay. To study the system, an EMT model is built and tested. FFT analysis is applied to derive the frequency distribution for both stable condition and boundary condition. To validate the system, an impedance-based model is derived and built based on grid side and controller side impedance. The simulation result shows that control delay could influence the HFOs and the negative damping of the system.

Acknowledgement

This project is supported in part by US Department of Energy grant DE-EE-0008771. The authors would like to acknowledge US Department of Energy Solar Energy Technology Office.

References

[1] C. Zou, H. Rao, S. Xu, Y. Li, W. Li, J. Chen, X. Zhao, Y. Yang, and B. Lei, "Analysis of resonance between a vsc-hvdc converter and the ac grid," *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10 157–10 168, 2018.

[2] H. Tao, H. Hu, X. Zhu, Y. Zhou, and Z. He, "Harmonic instability analysis and suppression method based on $\alpha\beta$-frame impedance for trains and network interaction system," *IEEE Transactions on Energy Conversion*, vol. 34, no. 2, pp. 1124–1134, 2018.

[3] C. Buchhagen, C. Rauscher, A. Menze, and J. Jung, "Borwin1-first experiences with harmonic interactions in converter dominated grids," in *International ETG Congress 2015; Die Energiewende-Blueprints for the new energy age*. VDE, 2015, pp. 1–7.

[4] Ł. H. Kocewiak, J. Hjerrild, and C. L. Bak, "Wind turbine converter control interaction with complex wind farm systems," *IET Renewable Power Generation*, vol. 7, no. 4, pp. 380–389, 2013.

[5] J. Zhu, J. Hu, L. Lin, Y. Wang, and C. Wei, "High-frequency oscillation mechanism analysis and suppression method of vsc-hvdc," *IEEE Transactions on Power Electronics*, vol. 35, no. 9, pp. 8892–8896, 2020.

[6] J. Man, L. Chen, V. Terzija, and X. Xie, "Mitigating high-frequency resonance in mmc-hvdc systems using adaptive notch filters," *IEEE Transactions on Power Systems*, pp. 1–1, 2021.

[7] C. Yoon, H. Bai, R. N. Beres, X. Wang, C. L. Bak, and F. Blaabjerg, "Harmonic stability assessment for multiparalleled, grid-connected inverters," *IEEE Transactions on Sustainable Energy*, vol. 7, no. 4, pp. 1388–1397, 2016.

[8] E. Ebrahimzadeh, F. Blaabjerg, X. Wang, and C. L. Bak, "Harmonic stability and resonance analysis in large pmsg-based wind power plants," *IEEE Transactions on Sustainable Energy*, vol. 9, no. 1, pp. 12–23, 2018.

[9] J. Sun, I. Vieto, E. V. Larsen, and C. Buchhagen, "Impedance-based characterization of digital control delay and its effects on system stability," in *2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2019, pp. 1–8.

[10] E. V. Larsen and J. Sun, "Managing resonances in windfarm collector systems," in *20th Wind Integration Workshop September 2021 and published in the workshop proceedings*, 2021, pp. 1–7.