

A Synchronphasor-Based SCADA Testbed

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Abstract—This paper presents the real-time hardware implementation of the supervisory control and data acquisition (SCADA) system in the Smart Grid Power Systems Laboratory at the University of South Florida. Opal-RT’s real-time simulator is employed to conduct power grid simulation and provide analog measurements in real-time. National Instruments’ Compact RIO (cRIO) and Open Source Data Concentrator (OpenPDC) are applied to realize real-time data acquisition and communication via the IEEE C37.118 protocol. The Control Center is programmed in National Instruments’ Single-board RIO (sbRIO). The Cascading Failure phenomenon and synchronphasor technology application are demonstrated.

Index Terms—SCADA, Real-time Simulation, Phasor Measurement Unit, Synchronphasor.

I. INTRODUCTION

A supervisory control and data acquisition (SCADA) System makes full use of the advanced communication technology to collect measurement data from the remote terminal units (RTUs) and phasor measurement units (PMUs) for monitoring and control [1]–[3]. Implementing a SCADA testbed in a research laboratory with a variety of hardware devices and software packages is challenging. The integration of measurement, communication, and control is the key to complete the testbed. Such a testbed can give an in-depth understanding of the composition of the real-world power system and its communication and control. On the other hand, such a testbed is closer to reality compared to a complete software and network-based PMU-based SCADA implementation in [2].

In this research, a SCADA testbed close to reality is built. It is capable of real-time data acquisition, monitoring, and control. The testbed is a hardware-in-the-loop (HIL) testbed. Compared to many HIL testbeds with the capability of both control and communication built in university research labs, e.g., the HIL testbed in Univ. of Illinois for microgrid control [4], the unique feature of this testbed is its adoption of PMU data for communication via the industry standard protocol C37.118. This paper presents the PMU-based SCADA testbed HIL design and the implementation challenges.

In this testbed, real-time simulation of large-scale power systems is carried out in the Opal-RT’s simulator to provide measurements for the SCADA System at real-time. National Instruments’ Compact RIO with a programmed PMU algorithm is employed to collect measurements from the power grid and transmit them to the next layer. Open-source Phasor Data Concentrator (OpenPDC) sets up the communication ports between the PMUs and the control center and also stores the streaming measurements to a structured query language (SQL) database. When the phasor measurements are delivered

to the control center, which is built in National Instruments’ single-board RIO, the phasor monitor will present the grid operation condition in real time.

For real-time communication, the grid measurements are collected by the PMU device via physical cables after scaling. From PMU to the Control Center, all communication is done through Ethernet among TCP ports under the IEEE C37.118 standard [5], [6].

The rest of the paper is organized as follows: Section II introduces the SCADA system with integrated components. The simulated power grid is discussed in detail in Section III. Section IV presents the PMU configuration and phasor-based communication technology. The control center is presented and the cascading failure phenomenon and synchronphasor-based control are demonstrated in Section V. Section VI gives the conclusion of the SCADA System’s implementation.

II. SCADA SYSTEM STRUCTURE

The structure for the implemented SCADA system is shown in Fig. 1. The power grid is emulated by Opal-RT’s RT-Lab simulator. Three-phase instantaneous measurements are taken from the selected buses and output as analog signals from RT-Lab. Measurement signals are sent to the PMU, which is implemented in National Instruments’ CompactRIO. Both parts are controlled by separate host PCs through ethernet connections.

After processing, the synchronphasor signals generated by the PMUs are transmitted to the OpenPDC. The real-time time-series data streaming, processing, and recording are realized via OpenPDC. Communication protocol applied is the IEEE C37.118 standard for synchronphasor measurements, which is dependent on Transmission Control Protocol (TCP).

To visualize the effect of the SCADA system, the synchronphasor signals are transmitted to another host PC acting as a control center. In the control center, a GUI for synchronous phasor measurements is built with National Instruments’ Single-board RIO and LabVIEW real-time control blocks. To demonstrate the system status and connection mode, a physical DC motor is connected to the system as a load in the power grid. When the system has no fault, the motor runs normally. When a fault is placed, the motor will experience a blackout situation and stop rotating.

III. REAL-TIME SIMULATION OF A POWER GRID

In this testbed, the power grid applied in the SCADA testbed is the IEEE 39-Bus system, which has been built in RT-Lab. Ten synchronous generators are modeled for dynamic

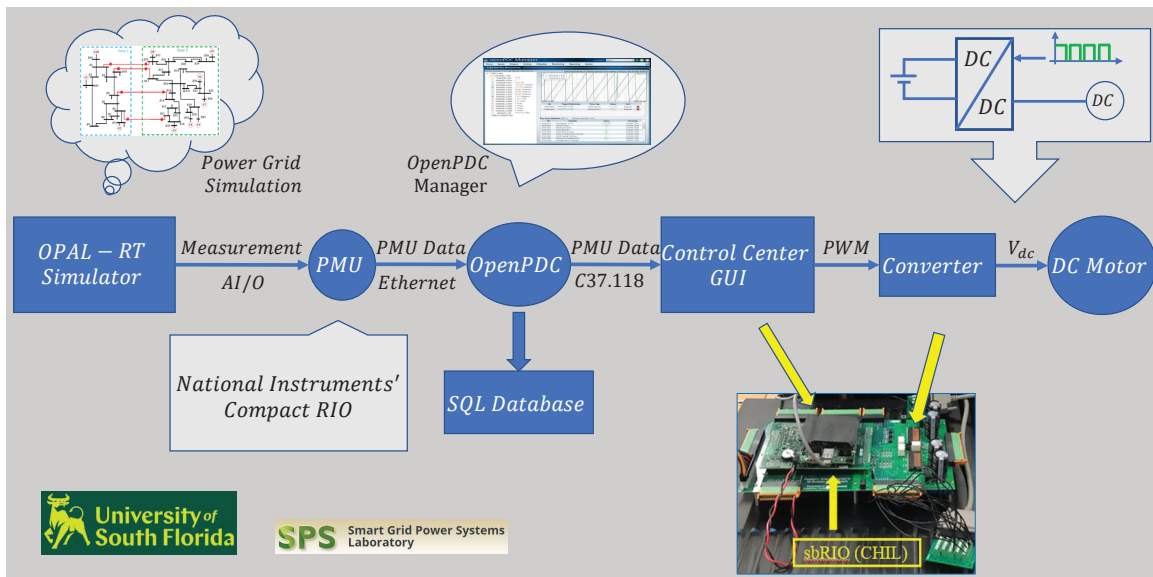


Fig. 1: Architectural structure of SCADA System.

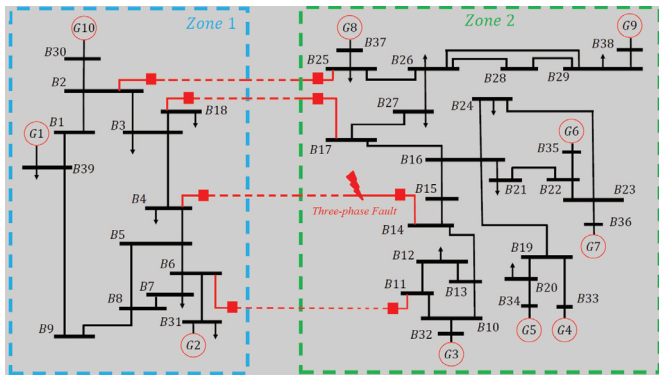


Fig. 2: Single-line view diagram of the IEEE 39-Bus System.

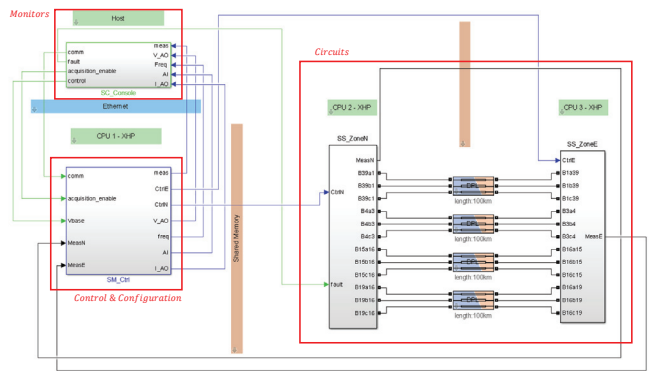


Fig. 3: RT-Lab model with subsystem arrangements.

simulation. The single-line view diagram of the IEEE 39-Bus system is presented in Fig. 2 [7], [8].

As shown in Fig. 2, the 39-Bus system is separated into two zones. Zone 1 and Zone 2 are connected by four transmission lines with breakers. A three-phase balanced fault is placed on the transmission line between Bus 4 and Bus 14. The protection system is also modeled in simulation. It keeps monitoring the three-phase voltage/current measurements and will send breaking signals when over-current is observed.

Fig. 3 presents the screenshot of the RT-Lab model interface. It includes a subsystem master for controller implementation, a subsystem console for monitoring, and two subsystem slaves for circuit implementation for Zone 1 and Zone 2 respectively.

The real-time simulator employed to run the grid simulation is Opal-RT's OP5600 equipped with 4 activated CPU cores at 3.0 GHz. In the RT-Lab model, each subsystem block, besides the subsystem console, will occupy one CPU core to decrease the computational burden under hardware synchronized real-time simulation mode.

The three-phase voltages are measured at certain buses and sent out to the PMU device through analog output ports. Since

the analog output range for OP5600 real-time simulator $\pm 16V$, so the measurement signals are scaled down first in simulation. Fig. 4 shows the RT-Lab hardware simulator and connection with a PMU device.

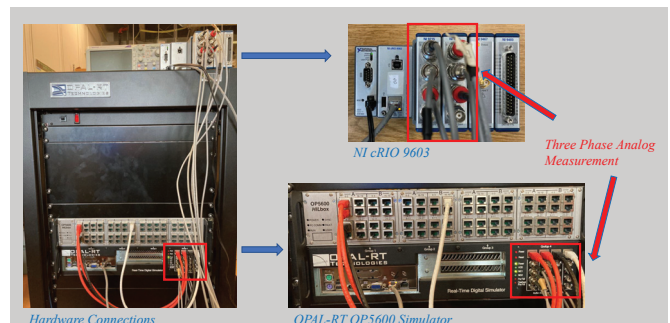


Fig. 4: Opal-RT OP5600 real-time simulator and the PMU device of the SCADA System. Three-phase voltage measurements in analog signals are transmitted to PMU AIO ports through cables.

IV. PMU-BASED COMMUNICATION

The PMU device used in the SCADA testbed is National Instruments' CompactRIO (cRIO-9063) and voltage I/O mod-

ules (NI-9215), shown in Fig. 4. The PMU function is realized by a LabVIEW program, virtual instrument (VI), with real-time and FPGA module. Modified LabVIEW VI is compiled with a local server and uploaded to the FPGA chip (Zynq-7020 FPGA) in the cRIO controller through Ethernet with the connection to the host PC. The interface of PMU VI is presented in Fig. 5.

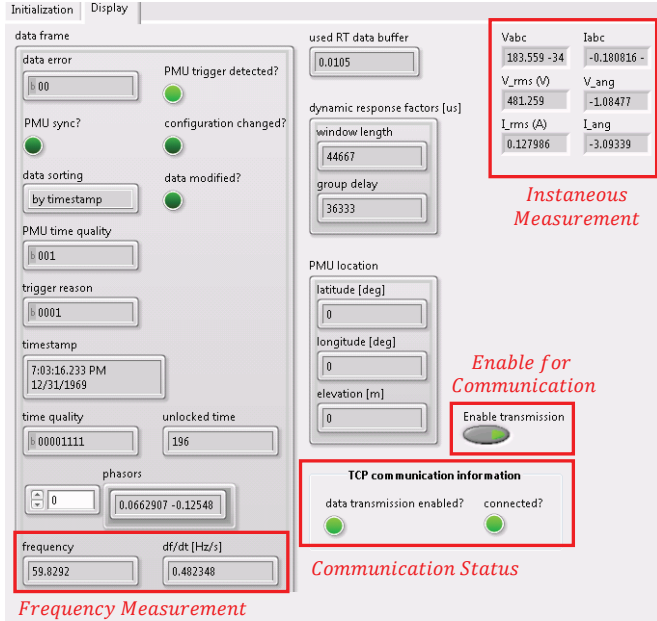


Fig. 5: LabVIEW VI GUI for PMU.

Three-phase voltage measurements are captured and re-sampled first. The measurements are then put on timestamps and converted into phasor measurements. The phasor measurement's data format follows C37.118 protocol format as synchrophasors. Through designed TCP port, the synchrophasor data is sending to the Data Concentrator.

Setting up the entire SCADA testbed requires testing for each component and procedure. Specifically, the real-time communication requires a connection test. The software, *PMU Connection Tester*, is applied to examine port availability and connection status [9]. When the connection is successfully set up, the PMU output port is occupied by the tester. Fig. 6 shows the received PMU data including frequency and phase angle.

A communication port is guaranteed as active after passing the tests using *PMU Connection Tester*. In order to ensure the Data Concentrator can receive the real-time synchrophasor measurements, the port needs to be released by disconnecting from the tester.

The Data Concentrator applied for real-time synchrophasor data streaming and storage is the OpenPDC by Grid Protection Alliance [10]. In the SCADA system, OpenPDC will first get the synchrophasor measurements and store them into an SQL database. OpenPDC is then prepared for user-defined actions as configured. Fig. 7 shows the selected signals from the streaming data of phase angle measurements.

From the graphic measurement scope, the phase angles are presented and indicated the correctness of connection and system operation condition. Next, the real-time data will be

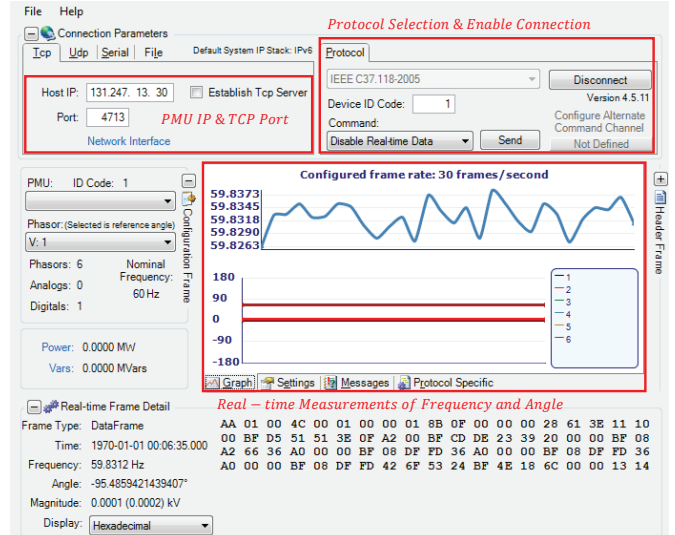


Fig. 6: GUI of PMU Connection Tester with real-time measurements. Real-time communication path is indicated as successfully connected.

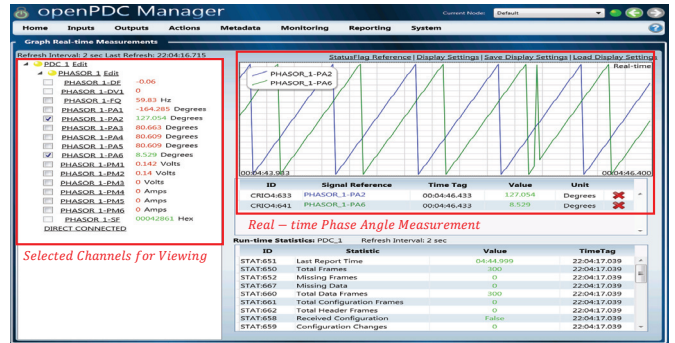


Fig. 7: Screenshot of the streaming graph measurements of two rotating phase angles in OpenPDC Manager.

uploaded to the Control Center of the SCADA system for operation purposes via Ethernet connection from TCP port.

V. CONTROL CENTER GUI

The control center of the SCADA testbed is implemented in the National Instruments' single-board RIO, which is a real-time processor with re-configurable Spartan-6 LX45 FPGA and 400 MHz CPU. Real-time synchrophasor measurement data are input into the control center with the relevant information, e.g., RMS values and phase angles, being extracted.

The main GUI of the control center is shown in Fig. 8. In the real-time monitor, the phasors of the three-phase voltage measurements from the selected buses are plotted in the phasor diagram.

The two buses are located on both sides of the transmission line in the IEEE 39-Bus power grid. When the system is stable, both voltage measurements are supposed to have close magnitudes, frequency, and phase angles. In the phasor diagram, both sets of phasor measurements are relatively static to each other. As the fault is placed, the system loses stability and the phasor measurements are no longer relatively static. The control center will react based on the relative position of phasor measurements and operates the grid.

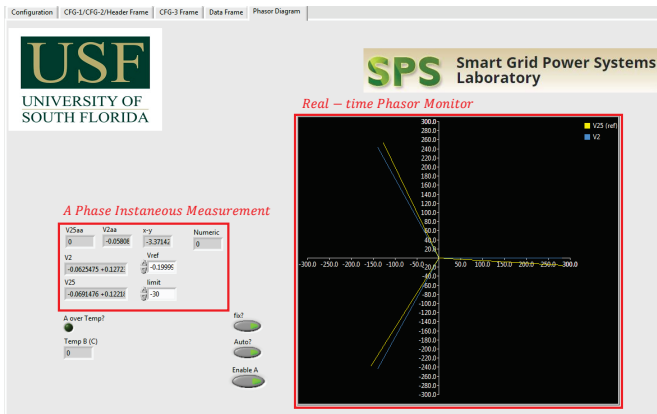


Fig. 8: Graphical User Interface of SCADA testbed Control Center.

Behind the control center, a DC motor is powered by a DC/DC converter which is controlled under the NI's Single-board RIO 9606. As previously mentioned, the motor can indicate the grid operation condition and directly show to the audience with rotation status. When the grid operates at normal conditions, the control center keeps sending a switching signal to supply the DC motor to indicate that the grid is stable. When fault happens, over-currents are observed and transmission lines are tripped, which causes the phasors to lose fixed relative position. Then control center senses the position change and stops the rotation of DC motor.

A. SCADA System Demonstrations

The demonstrations presented in this paper includes the two major components, the cascading failure phenomenon and synchrophasor-based fault detection [11], [12].

In Fig. 2, a three-phase fault is placed on the transmission line between Bus 4 and Bus 14. The line current immediately exceeds the design limit and triggers the relay to trip the line. Due to the loss of a transfer path between Zone 1 and Zone 2, the other 3 lines compensate by increasing their current flows, which gradually cause over-currents. In turn, the rest of the transmission lines between two zones are tripped one after the other until the Zone 1 and Zone 2 are completely separate. The sequential line tripping process demonstrates the cascading failure in the power system.

To visualize the cascading failure phenomenon, the three-phase current measurements on the 4 transmission lines are collected in real-time from RT-Lab simulation in Fig. 9. Based on recorded data, the fault is randomly applied at 64.97 s, and current measurement taken from Bus 14 shows sudden increase and exceeds the limit. The line is then tripped. The second line experiences tripping after 0.83 s according to current measurement at Bus 6. Next tripping line is between Bus 17 and 18, which happens 1.44 s after fault. The last line was tripped 1.87 s after fault between Bus 2 and Bus 25.

Fig. 10 shows the time-domain measurements of A phase voltage at Bus 25 and Bus 2 captured by RT-Lab meanwhile the demonstration is running. From the measurements, it can observe that cascading failure causes line tripping at around 66.8 s. After line tripping, voltages start to recover, however,

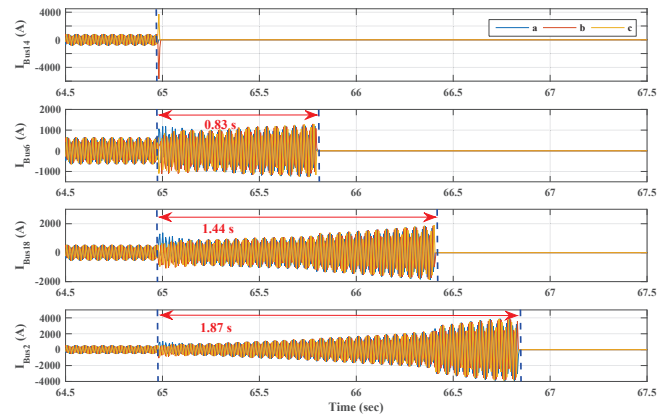


Fig. 9: Cascading failure due to fault on transmission line between Bus 4 and 14. (A.) Line between Bus 4 and Bus 14 was tripped immediately. (B.) Line between Bus 6 and 11 was tripped 0.83 s later. (C.) Line between 17 and 18 was tripped 1.44 s after fault. (D.) Line between Bus 2 and 25 was tripped 1.87 s after fault. Zone 1 and Zone 2 are completely separated.

the phase angles of the two zones can no longer be close to each other. The second plot shows that Bus 2 voltage is almost identical to Bus 25 voltage before the fault happens at around 64.97 s. And after line tripping, Bus 2 voltage and Bus 25 voltage show larger difference on magnitude and phase angle in the bottom plot. As the time-domain results demonstrated,

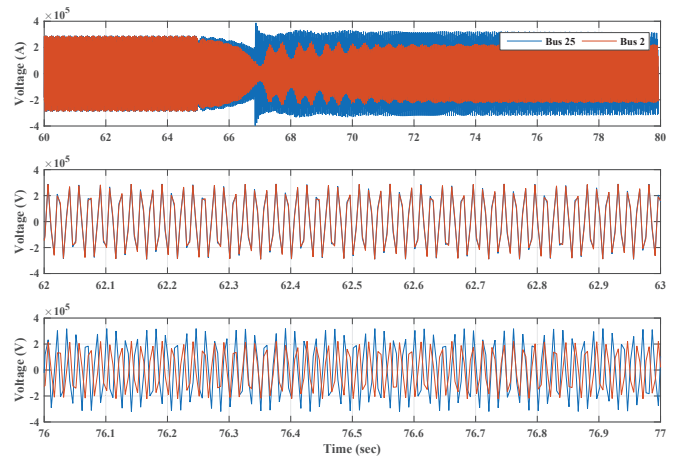


Fig. 10: Time-domain Phase A voltage measurements at Bus 25 and Bus 2.

we expect to see phasor diagram shows the relative position is no longer static.

In the control center, real-time voltage measurements on Bus 2 and Bus 25 are monitored. After fault and cascading failure, the relative position of the phasors starts to change significantly. The comparison of voltage phasor diagram before and after fault is presented in Fig. 11. In the monitor, Bus 2 voltage phasor is set as default and its A phase component is fixed at 0 degree. Bus 25 voltage phasor is relatively static to Bus 2 voltage before fault, and then its magnitude and phase angle start to change due to system instability.

When the system lost synchronism, the voltage phase angle difference between the two zones exceeds a threshold. The control center then sends out a signal to the DC motor's DC/DC converter to stop the DC motor.

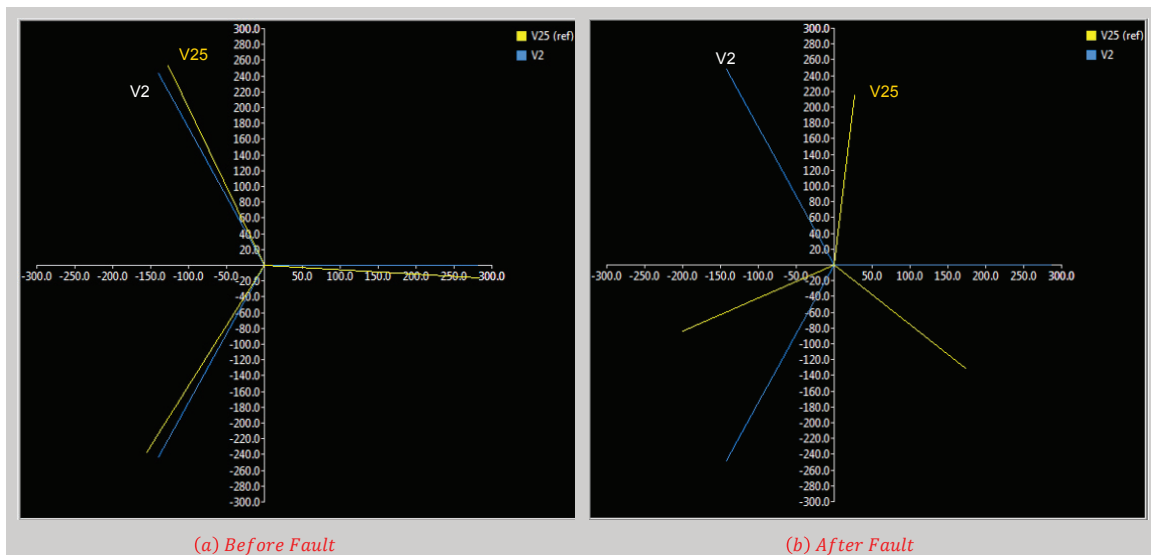


Fig. 11: Comparison between the real-time phasor diagrams. Diagram (a) shows the voltage phasors at Bus 2 (blue) and Bus 25 (yellow) are relatively static and the system is stable. Diagram (b) shows the voltage phasors' relative position changes significantly and indicates the stability is lost.

VI. CONCLUSION

A PMU-based SCADA system HIL implementation is implemented as a university lab. This testbed demonstrates power system cascading failure and synchrophasor-based monitoring and control. The RT-Lab real-time simulator acts as the power grid and provides the real-time analog measurements for the PMUs. NI's cRIO 9063 is employed as a PMU device to collect instantaneous measurements, convert them into phasors, and send out phasor data in a format specified by C37.118 standard in real-time. An OpenPDC receives the PMU data and further transmits the data to the supervisory control center (implemented in NI's Single-board RIO 9606). Finally, the control center can send commands to operate a DC motor to indicate grid performance condition based on synchrophasor data received in real time.

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