Grid Forming Inverter: Laboratory-Scale Hardware Test Bed Setup and Weak Grid Operation

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***Abstract*—In recent times, the concept of grid forming inverters has gained popularity. Grid forming inverters have proven to be a promising alternative to the grid following inverters. In this paper, we present the hardware test bed implementation of grid forming inverter in islanding mode as well as in grid connected mode. The control structure includes inverter-level inner current control and outer voltage control, and plant-level $P-f$ and $Q-V$ droop control. The $Q-V$ droop provides the voltage command, whereas $P-f$ droop provides the frequency command and is also key for the synchronization process. While it is straightforward to set up the test bed for the islanded operation, it is a challenging process to set up the grid-forming inverter in the grid-connected mode. We present the key technologies and demonstrate the start-up process and weak grid operation using the hardware experiment results. Results from EMT model developed in MATLAB/SimPowerSystems are also presented for side-by-side comparison.**

***Index Terms*—Grid forming control, weak grid, droop control, synchronization**

I. Introduction

In recent times, the conventional power grid is quickly transitioning toward inverter-based resources (IBRs). For instance, in 2018, the Muai region in Hawaii reached 76% instantaneous penetration levels of IBRS, and the region is aiming towards 100% by the year 2045 [1], [2]. Generally, these IBRs are grid following inverters (GFL), where the control strategy is based on the assumption of the presence of a stiff grid. The control structure for the GFL inverter is based on phase-locked-loop (PLL), which enables proper tracking of voltage at the point of common coupling (PCC) bus and a healthy synchronization of the IBR to the grid. Over the years, the research paradigm has shifted towards a different type of IBRs known as grid forming inverters (GFM) [3], as an alternative to GFL controls. Conceptually GFM imitates a voltage source, which controls the voltage output and its frequency. Unlike GFL, GFM based control strategy does not rely on a PLL for synchronization (or voltage-based synchronization), rather rely on power-based synchronization [4]. Over time, various GFM control structures have been proposed [5]–[8].

In this paper, our focus is to implement the GFM inverter using laboratory-scale hardware test bed. Two test beds are developed for the grid forming inverter 1) islanding mode and 2) the grid connected mode. The control algorithms include inner current control, outer voltage control and droop control. The hardware test bed consists of a three-phase voltage source converter, real-time controller from Opal RT, and measurement units. Opal RT's RT-Lab software platform is used to implement the control structure in real-time. The EMT studies are performed in MATLAB/SimPowerSystems environment.

The rest of the paper is organized as follows. Section II describes the system topology and the control structure. Section III defines the hardware test bed. Section IV details the hardware implementation. Section V concludes the paper.

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II. System Topology

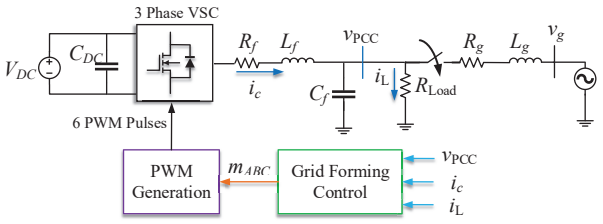

Fig. 1: System topology of grid connected system with grid forming control.

Fig. 1 presents the schematic diagram of the system. A three-phase voltage source converter (VSC) is connected to a purely resistive load (R_{Load}) at the point of common coupling (PCC) when operating in islanding mode and is connected to the grid through a transmission line when operating in grid connected mode. A series RL circuit represents the transmission line, where R_g and L_g are the resistance and inductance for the transmission line respectively. A RLC choke filter is connected at the terminal of the VSC with R_f, L_f, and C_f as the resistance, inductance, and capacitance respectively. A DC voltage source (V_{DC}) is connected at the DC terminal, and C_{DC} is DC-link capacitor.

The control algorithm for the system is based on the work presented in [9], [10]. The control is implemented in the grid's dq frame of reference. The following notation are used: i_{cdq}, v_{dq} and i_{Ldq} are the current flowing through the filter inductor (L_f), voltage at the PCC bus and the load current in dq frame respectively. P and Q are the real and reactive power at the PCC bus, and the per-unit expressions are :

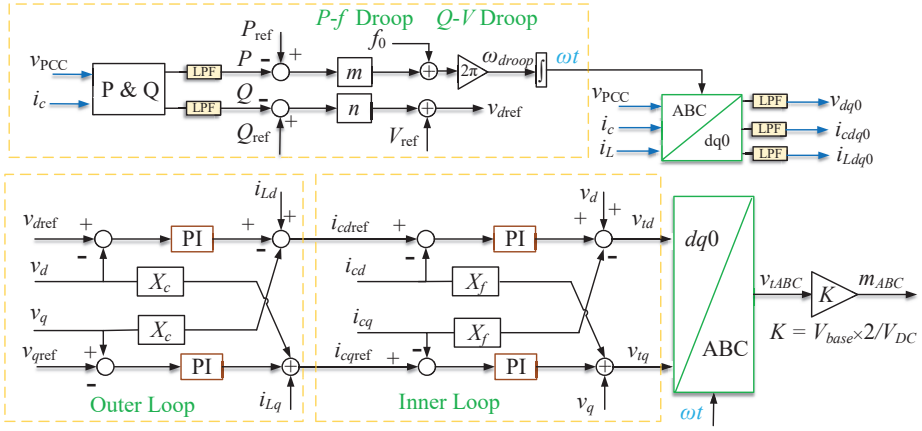

Fig. 2: Block diagram of the control structure adopted for grid forming inverter.

$$P = v_d i_{cd} + v_q i_{cq}$$
$$Q = -v_d i_{cq} + v_q i_{cd} \quad (1)$$

The inner loop is PI controller-based current control structure, where the filter inductor current (i_{cdq}) as the control variable. The PI controller gains for the inner loop are notated as k_{pi} and k_{ii}. The outer loop regulates the voltage at the PCC bus (v_{dq}), Similar to the inner loop, PI controller is used in the outer loop with PI gains k_{pv} and k_{iv}. Two droop control methods are implemented: (1) $Q-V$ droop and (2) $P-f$ droop.

$Q-V$ droop regulates the reactive power at the PCC bus and generates the d-axis reference signal (v_{dref}) for the outer loop. On the other hand, the $P-f$ droop regulates the PCC bus's real power and provides the desired angle (ωt) for the control. This droop acts as a synchronization unit in the absence of a dedicated phase-locked loop when the system is in grid connected mode. The droop gains are n and m for $Q-V$ droop and $P-f$ droop respectively. A suitable low pass filter is used to filter out unwanted harmonics. The control algorithm outputs three phase sinusoidal reference signals m_{abc} used for generation of the PWM pulses. A detailed block diagram of the control structure is presented in Fig. 2. Parameters for the two modes are listed in Table I. **Note:** The PI controller gains are based on per unit system.

A. PI Controller Parameters Selection

Selection of PI controller gains for the inner loop and the outer loop is an important step to ensure stable operation of the VSC systems. Poor selection of the control parameters may lead to undesirable operation or instability. While operating in grid connected mode, poor gains may lead to high transients during start-up process, and may lead to unstable system. Along with stable start up, we also desire to push maximum amount of power from the converter side to the grid side. In this section we discuss in brief about the transfer functions

TABLE I: Parameters used for grid forming inverter.

Description	Parameter	Value	
Power Base	S_b	50 VA	
Voltage Base	V_b	20 V (L-L rms)	
Nominal Frequency	f_0	60 Hz	
Grid Voltage	V_g	11.5 V (L-N, rms)	
DC Voltage	V_{DC}	40 V	
DC Link Capacitor	C_{DC}	260 μF	
Choke Filter	L_f, R_f, C_f	1.5 mH, 70 mΩ, 47 μF	
Transmission Line	R_g, L_g	0.2 Ω, 7.5mH	
Load	R_{Load}	20 W	
Switching Frequency	f_{SW}	5 kHz	
Control Parameters			
		Islanding	Grid Connected
Inner Loop Control	k_{pi}, k_{ii}	1, 10	1, 5
Outer Loop Control	k_{pv}, k_{iv}	0.2, 5	3, 50
Droop Parameters	m, n	0.05, 1	0.08, 0.1

for the inner loop and the outer loop [9], and their respective bandwidths.

1) Inner Loop: The closed loop transfer function for the inner loop is defined as:

$$G_{\text{inner}}(s) = \frac{G_{\text{open},i}}{1 + G_{\text{open},i}} \quad (2)$$

Here, $G_{\text{open},i}$ is the open loop transfer function, and is represented as:

$$G_{\text{open},i}(s) = \frac{k_{pi}s + k_{ii}}{L_{fpu}s^2 + R_{fpu}s} \quad (3)$$

The simplified block diagram is presented in Fig. 3.

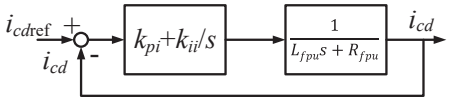

Fig. 3: Simplified block diagram for d axis inner loop current control.

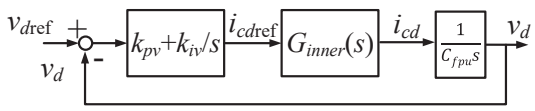

Fig. 4: Simplified block diagram for d axis outer loop voltage control.

2) Outer Loop: Similarly, the close loop transfer function for the outer loop is given by:

$$G_{\text{outer}}(s) = \frac{G_{\text{open},v}}{1 + G_{\text{open},v}} \tag{4}$$

Here $G_{\text{open},v}$ is the open loop transfer function, and is given by:

$$G_{\text{open},v}(s) = \frac{k_{pv}s + k_{iv}}{C_{fpu}\tau_i s^3 + C_{fpu}s^2} \tag{5}$$

It should be noted that $R_{f,pu}$, $L_{f,pu}$ and $C_{f,pu}$ are the per unit values of the RLC filter.

3) Bandwidth: From expressions presented in (2) and (4) bandwidths are estimated. Parameters used for calculating the bandwidths are listed in Table I. For islanding mode, the bandwidth for inner loop is 841 Hz and for the outer loop is 98 Hz. When the system operates in the grid connected mode, the bandwidths for the inner loop and the outer loop are 840 Hz and 1415 Hz respectively.

III. Hardware test bed

To emulate the system presented in Fig. 1 and Fig. 2 in real-time, a hardware test bed was established. The hardware components are explained as follows.

1) DC Power Supply: The DC voltage is provided to the VSC system with the help of BK Precision DC regulated power supply, model 1666. The maximum allowable voltage from the device is 40 V, and the current is 5 A.
2) Power Gird: The power grid source is emulated by Chroma Regenerative Grid Simulator 61845. The rated 3 phase power of the simulator is 45kVA, with a rated output voltage as 300 V(L-N). The Chroma simulator is controlled remotely with the help of LabVIEW installed on a host computer. The host computer and the simulator communicate with each other with the help of a GPIB cable.
3) VSC system: To arrange a three-phase VSC system, Imperix's power module PEB 8024 is used. PEB 8024 is a half-bridge power module featuring two Silicon Carbide (SiC) MOSFETs switches. Three individual PEB 8024 modules are connected to make one three-phase VSC. The power module consists of onboard with DC voltage sensor and current sensors and necessary over-voltage and current protections. The MOSFETs receive the gating pulses via an optic fiber connection.
4) Analog Sensor Units: The onboard current sensors embedded on the imperix power modules measures the three-phase current flowing in the filter inductrors. The voltage at the PCC bus and the current flowing in the load are measured by Opal RT's OP8662, a high voltage and current measurement unit.
5) Real-Time Controller: Opal RT's OP4500 acts as a real-time controller. The OP4500 acquires all the measured analog signals from different sensor units. The control algorithm is implemented and executed in OP4500 with the help of RT-Lab. The controller outputs the required PWM signals using digital out channels.
6) Power Interface: Opal RT's power interface allows to control of the imperix power modules with OP4500. The PWM signals generated by OP4500 are fed to the power interface, and are relayed to the imperix's power modules with the help of optic fiber cables.

Fig. 5 presents the hardware test bed for the grid forming inverter. When operating in islanding mode, the Chroma grid simulator and the transmission line (red-dotted box) are not connected to the system.

IV. Hardware Implementation

Laboratory level hardware implementation is a crucial step in understanding various control algorithms and system interactions in real-time. They are also provide a very high degree of validations of observed phenomenon's in simulations. The schematic of the hardware test bed is presented in Fig. 5, and has been already discussed in section III. Here, we present two experimental studies (a) when the system is in Islanding mode (b) when the system is in grid connected mode.

A. Islanding Mode

The hardware test bed for the islanding mode is presented in Fig. 5 (without the grid simulator and transmission line). For the real-time implementation, control structure is enabled in steps. First, we operates with open loop controller, sinusoidal PWM technique (SPWM), with the amplitude of the modulation signal as 0.8. At t = 16s, we enable the outer loop and the inner loop simultaneously, with $v_{d\text{ref}}$ = 0.8 pu, while keeping $v_{q\text{ref}}$ = 0 pu. At $t = 23$ s, we change $v_{d\text{ref}}$ = 1.0 pu, and the system quickly follows the reference command. At $t = 30$ s we enable the droop controls ($P - f$ droop and $Q - V$ droop). For droop control we provide P_{ref} = 0.4 pu, Q_{ref} = -0.14 pu, and V_{ref} = 1 pu. The results are presented in Fig. 6. The parameters used for islanding mode are tabulated in Table I.

B. Grid Connected Mode

Next, we implement the system in grid connected mode, as shown in Fig. 5. The control structure is exactly same as the islanding mode. Here, we discuss energizing process of the VSC system, system behavior in weak grid conditions, and key learning from the experiments. The parameters used for the hardware implementation and simulation studies are listed in Table I.

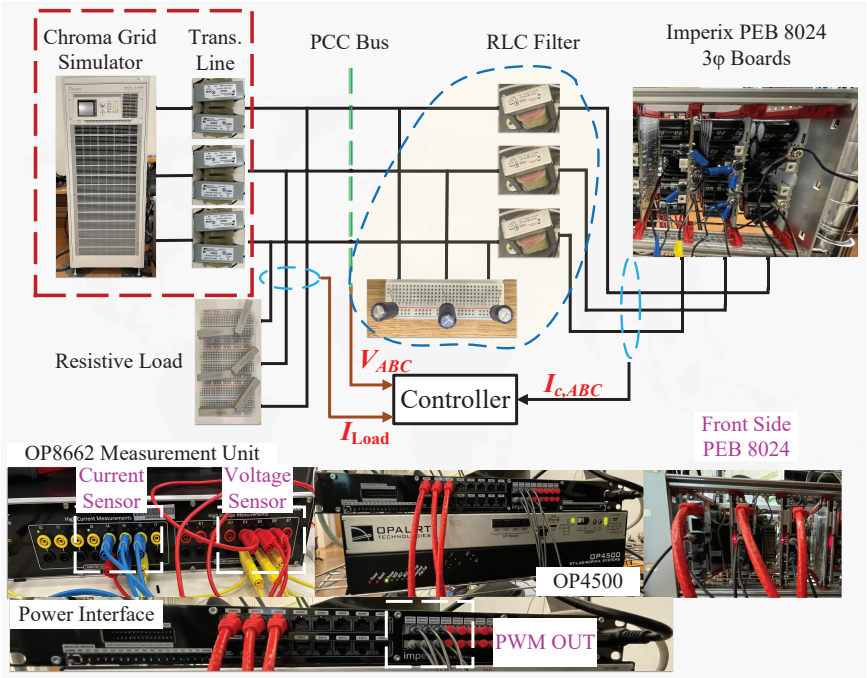

Fig. 5: Laboratory-scale hardware test bed for implementing grid forming inverter.

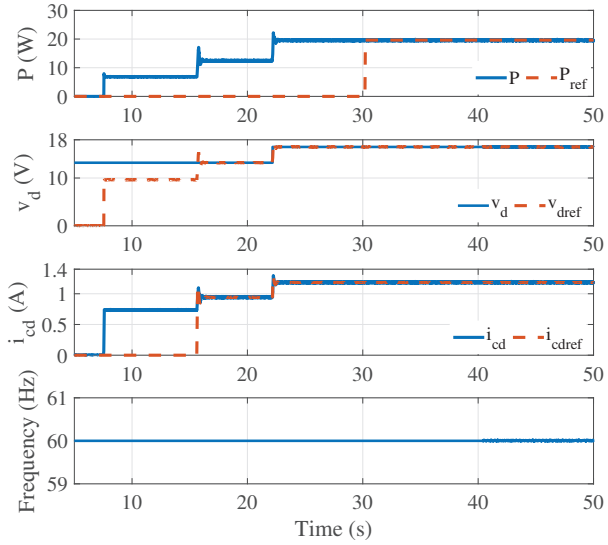

Fig. 6: Experimental results obtained from hardware test bed when the system operates in islanding mode. 0-5 s: PWM signal blocked. $t = 5$ s: open-loop modulation enabled. $t = 16$ s: inverter-level control enabled. $t = 30$ s: plant-level droop control enabled.

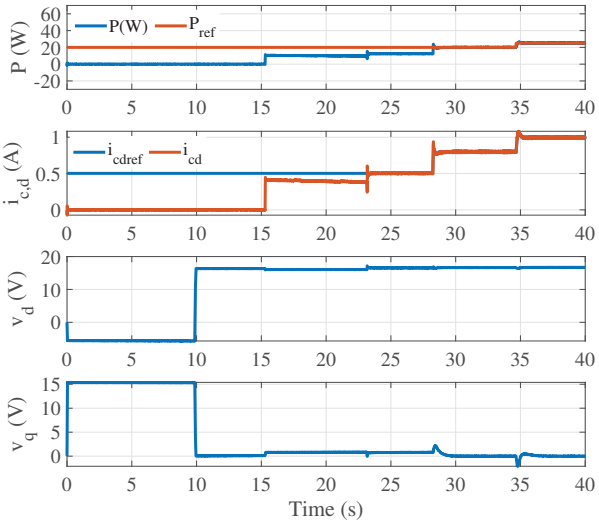

Fig. 7: Experimental results presenting energizing process and synchronization of the VSC system to the grid. $t = 15$ s, PWM signal unblocked and open-loop control enabled. $t = 23$ s, inner current control enabled. $t = 28$ s, all-level control enabled.

1) Energizing: One of the significant steps while operating on the VSC system was to ensure that the power flow direction was always from the VSC to the grid since the DC side power supply did not have the power absorbing capabilities. Therefore, the grid voltage angle (notating as θ_g) should always be less than PCC bus angle (notating as θ_{PCC}). Unlike the simulations where the assumption is that the grid is always at 0° and 60 Hz might not be true in the real-time.

Hence, to ensure the power always flows towards the grid, the VSC system was energized in various steps and are discussed in context to Fig. 7.

Step 1 included blocking the PWM signals to the VSC and switching on the grid simulator and the DC voltage source. The voltage signal at the PCC bus is observed and the magnitude and the initial phase angle (notating it by θ_{PCC0}) information

is collected. The angle information is manually entered in the control, and is necessary for proper abc-$dq0$ transformations. Also, since very less current flows during step 1, it is safe to assume that $\theta_{\text{PCC0}} \approx \theta_g$.

In Fig. 7, the time period from t = 0 s to t = 15 s, we operate in step 1. At t = 10 s, we enter the θ_{PCC0} information, and we can see that v_d changes from -5.5 V to 16.32 V, where as v_q changes from 15.31 V to 0 V. This initial phase angle θ_{PCC0} is important to ensure that the control is in proper frame of reference.

In **Step 2**, we operate the system with open loop control. SPWM technique is implemented to control the VSC system while in open loop control. As discussed earlier, the major task is to ensure power flows towards the grid. Hence, the initial phase angle of the sinusoidal reference signal for PWM generation is properly assigned, and is allocated higher than θ_{PCC0}. For example, $m_{a,\text{open}}$ is phase A reference signal, is presented as:

$$m_{a\text{open}} = M \sin(\omega_o t + \theta_{\text{open}}) \tag{6}$$

Here, M is the peak value of the sinusoidal signal and θ_{open} the phase angle, and $\theta_{\text{open}} > \theta_{\text{PCC0}}$. It was found that if θ_{open} = θ_{PCC0} + 10°, no reverse flow of power was encountered. At around t= 15 s, we enable the PWM signals and turn on the open loop control. We can see a smooth integration of the VSC to the power grid.

For **Step 3**, we enable the inner current control loop, keeping $i_{cd\text{ref}}$ = 0.5 A and $i_{cq\text{ref}}$ = 0. The inner loop is enabled at t = 23 s. The system quickly follows the reference commands.

Step 4 is the last step in energizing the VSC system, completes the proper synchronization process. Here, we enable the droop control and the outer loop voltage control simultaneously. The reason for enabling droop and the outer loop together will be discussed subsequently. At t = 28 s both

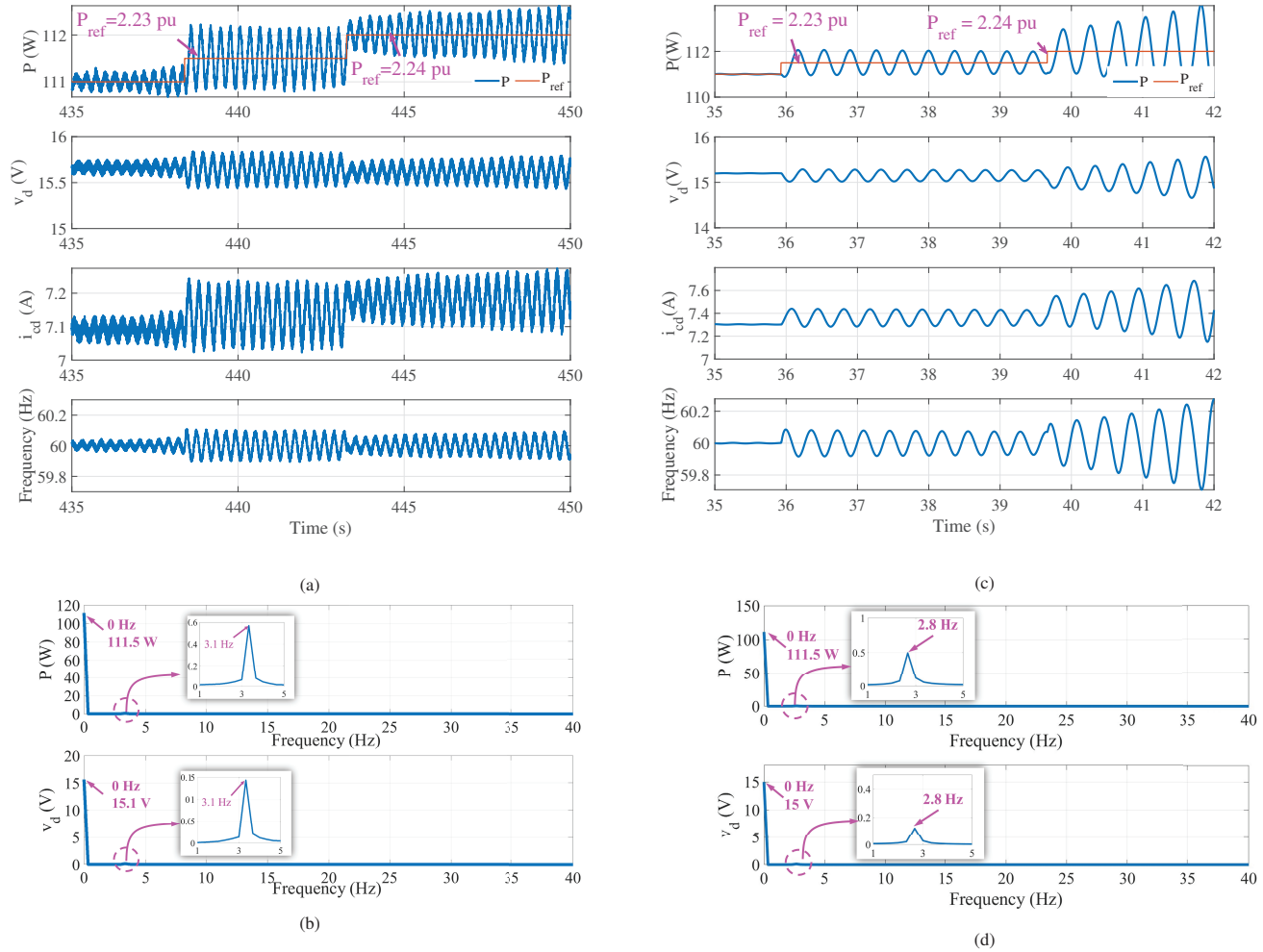

Fig. 8: Hardware test bed (a,b) and EMT simulation test bed (c,d) results. (a,c) Time-domain responses of real power P (W), d-axis PCC bus voltage v_d (V), d-axis choke filter current i_{cd} (A) and frequency (Hz), when P_{ref} is increased. In the hardware test-bed, the switching frequency of the SiC switches is 5 kHz. In the EMT simulation, average model is adopted for the simulation studies. (b,d) FFT results.

control loop are enabled, with P_{ref} = 20 W (0.4 pu). At t = 34.75 s we again change the P_{ref} = 25 W (0.5 pu). For both cases, the system follows the control command efficiently. This completes the energizing and synchronization process of the VSC system to the power grid.

2) Weak Grid Operation: The hardware test bed is used to study the VSC system under weak grid conditions in real-time. P_{ref} is increased in steps, and the system response is recorded in real-time. Similar case study and analysis were also conducted using MATLAB/SimPowerSystems. The time domain results for both the cases are presented in Fig. 8. It is observed from Fig. 8 that when P_{ref} is increased the system is subject to low frequency oscillations. In addition to that, the system losses its stability when P_{ref} = 2.24 pu, with P_{ref} = 2.23 pu being the marginal condition.

Fast Fourier Transform (FFT) was performed to obtain the frequency of the oscillations. For both, the real-time implementation and simulation studies, the frequency of oscillations was $\approx$ 3 Hz. Fig. 8 presents the magnitude spectrum for the real power P and the d-axis PCC bus voltage v_d.

3) Key Learning: As mentioned earlier in the real world the grid voltage might not always be at ideal conditions, such as at 0° phase angle and at 60 Hz. Unlike grid following control structures, where we have PLLs to synchronize the VSC to the grid, grid forming control lacks a dedicated synchronization unit. Hence, the $P-f$ droop is required to ensure the proper synchronization of the VSC to the grid, and is also termed as power synchronization [5]. In power synchronization, the VSC system synchronism with the grid by the virtue of transient power transfer [11].

Fig. 9 presents a case where the droop control is not implemented, and the system operates with just outer loop and inner loop. We enable the outer loop at t=75 s. It is noted from Fig. 9 that the signal v_q is not stable and is increasing linearly with a positive slope. Hence, when the outer loop is enabled, the measurement fails to follow the reference command. If operated further, the system losses its stability.

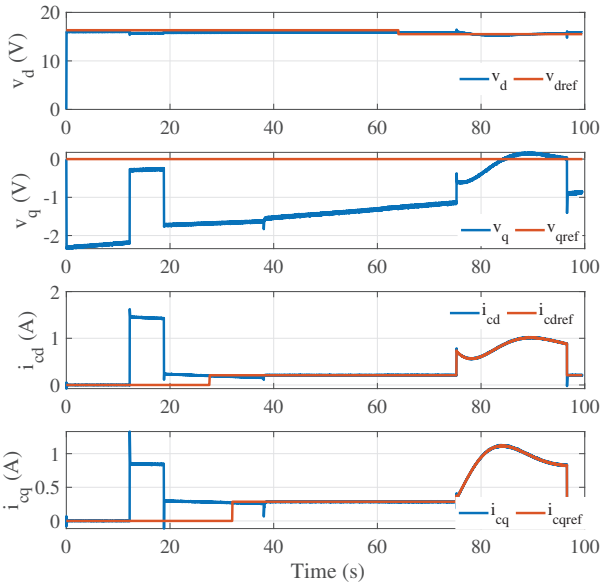

Fig. 9: Experimental results for the case when $P-f$ droop is not implemented for synchronization.

V. CONCLUSION

In this paper we studied the grid forming inverter with the help of laboratory-scale hardware test bed. The system was operated in islanding mode as well as grid connected mode. In the grid connected mode, we demonstrate the start-up process of the VSC system, and the system behavior under weak grid conditions. From the experimental results we observe low-frequency oscillations when more power from the converters side to the grid side. Results from the EMT simulations are also presented for side-by-side comparison.

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