Modeling and Control of Grid-following Single-Phase Voltage-sourced Converter

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***Abstract*—This paper presents the modeling of grid-following single-phase voltage-sourced converter (VSC). The electromagnetic transient (EMT) simulation is carried out via MATLAB/Simulink with SimPowerSystems Toolbox. Detailed IGBT switches are included in the DC/AC inverter model. Second-order generalized integrator-based Phase Locked Loop (SOGI-PLL) is implemented for synchronization and the dq-components extraction purposes. Real and reactive power control is implemented for converter operations. Multiple grid dynamic events are designed in the simulation testbed for analysis and demonstration.**

***Index Terms*—Single-phase VSC, Grid-following, SOGI, PLL.**

I. Introduction

The penetration of inverter-based renewable energy resources significantly increases recently and the control of inverter becomes a critical topic in the renewable energy research field. Three-phase VSCs and control have been introduced by many textbooks [1]–[3] and many researches have been developed [4], [5].

Compared to the three-phase VSC study, researches on the single-phase VSC have been less conducted. The major difference is the control of the single-phase VSC. In three-phase system, the Park Transformation or abc/dq transformation with the phase angle generated by reference or estimated by PLL in grid forming and following connection can easily extract direct-quadrature components from three-phase measurement for control purposes.

The key of controlling the single-phase VSC is to extract the direct-quadrature components. For a constant frequency system, the variable time delay method can be simply applied to obtained a component with 90 degree shift, which is similar to the Clarke Transformation [3]. However, such an ideal system cannot handle the grid frequency change. The adaptive methods to achieve decomposition usually required feedback loops [6]–[8]. Additionally, the single-phase PLLs are also different in structure [9]–[11].

In this paper, an electromagnetic transient simulation testbed of a grid-following single-phase converter has been built and presented. The second-order generalized integrator-based transformation and PLL are implemented for the measurement processing and inverter synchronization [3], [11].

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As a grid-following inverter-based system, the connection and the grid side operation condition are significantly important to the inverter control and performance. Thus, three major dynamic events are designed and demonstrated in the case study based on the same simulation testbed. The first event is the weak grid connection, which is caused by an increasing transmission line reactance. The second and third events are emulating system dynamic responses to the changes of grid side voltage magnitude and frequency. To benchmark, power flow-based steady state analysis and system initialization is performed via a formulated optimization problem with YALMIP [12]. The limits of the system to handle weak grid and grid voltage changes are also solved in advanced and verified in the EMT simulation.

The rest of the paper is organized as follows. Section II introduces the detailed implementation of the gird-following single-phase VSC testbed, including circuit, SOGI-PLL, control logic, and steady state analysis. The case studies of the PLL performance, ripple frequency analysis, and dynamic events are presented in Section III. Finally, Section IV gives the conclusion.

II. Single-phase Grid-following VSC Testbed

A. Circuit Topology

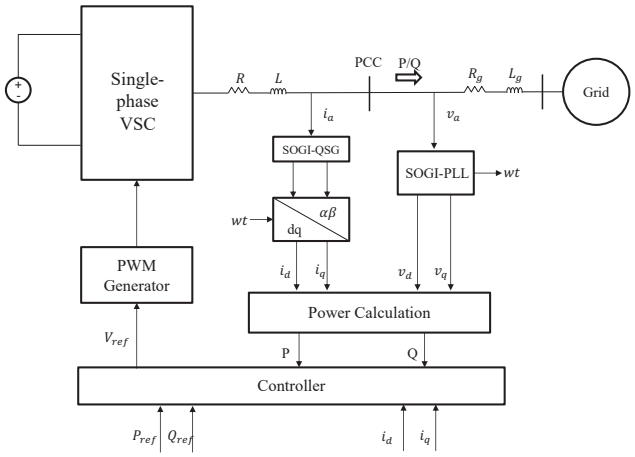

Fig. 1: Single line topology of the circuit.

The study system is shown in Fig. 1. A single-phase VSC is connected to the grid voltage through an RL filter and transmission line. The point of common coupling (PCC) bus is connected after the RL filter for single-phase voltage and current measurements.

PCC bus measurements are collected and sent to the controller. PLL is applied to generate phase angle information from voltage measurement for synchronization and dq-frame decomposition purposes. For the single-phase study system, a second-order generalized integrator-based PLL is employed. The real and reactive power are computed from voltage and current dq-components and fed into the control algorithm. In the end, the reference signal is fed into a 2-level bipolar PWM generator for inverter switching control. Table. I shows the system parameters.

TABLE I: Parameters of the main system

Item	Value	Item	Value
S_{base}	4000 VA	V_n	190.52 V
R	1.1E-5 *pu*	X	1.142 *pu*
R_g	0.05 *pu*	X_g	0.25 *pu*

B. Phase Locked Loop

According to [3], the SOGI-PLL is implemented in the testbed. The block diagram of the structure is shown in Fig. 2. Compared to conventional PLL, the SOGI-PLL has a quadrature signal generator (QSG) in front of the Park Transformation, which requires the estimated frequency to be returned for $\alpha\beta$-components extraction.

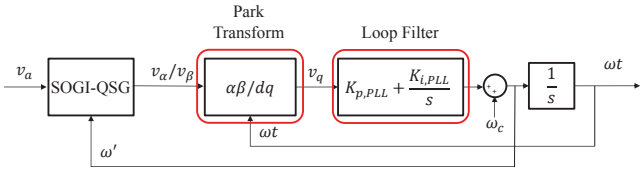

Fig. 2: Block diagram of Second-order Generalized Integrator-based Phase Locked Loop (SOGI-PLL).

Fig. 3 presents the structure of SOGI-QSG in detail. v_a is the single-phase AC voltage measurement from PCC bus and sent into the SOGI-PLL as input. The estimated $\alpha\beta$-components, v_α and v_β, are the outputs of the QSG. Note the v_α and v_β are 90 degrees apart, and v_α is the same as input signal at steady state.

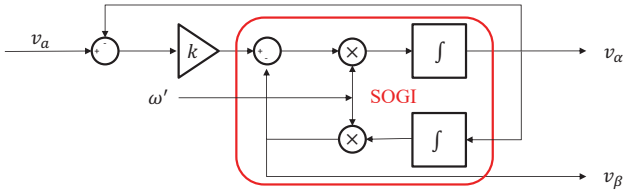

Fig. 3: Structure of SOGI for quadrature signal generation.

With extracted $\alpha\beta$-components, the Park Transformation is applied to gather dq-frame components, v_d and v_q. The transformation is done through the following computation process.

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{1}$$

The loop filter is a PI controller with input of v_q extracted from Park Transformation. The DC value will be pushed to zero while PLL is tracking the angle. In results, the v_d is equal to the voltage amplitude and v_q is equal to 0. At steady-state, the estimated phase angle is locked up with the input and outputted as ωt, which is applied to extract current dq-components and the reference signal generation for the PWM generator with Inverse Park Transformation. The gain applied in the implemented SOGI-PLL is presented in Table. II.

TABLE II: Parameters of SOGI-PLL

Item	Value	Item	Value
$K_{p,PLL}$	60	ω_c	376.9 rad/s
$K_{i,PLL}$	1400	k	$\sqrt{2}$

C. Control Algorithm

In the presented testbed, the control algorithm is shown in Fig. 4. The inner control loop is current control with decoupling feed-forwards. And the outer control loop is real/reactive power control. Controller reference frame is based on the PCC bus phase angle.

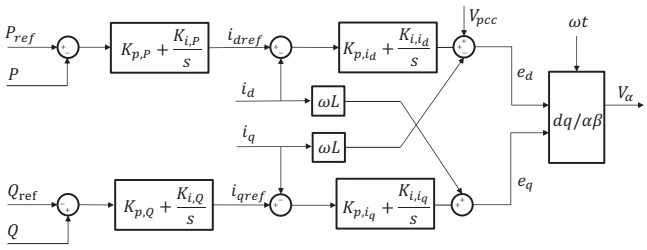

Fig. 4: Block diagram of the inverter control. Inner loop is current control. Output loop is real/reactive (P/Q) power control.

For the dynamic real/reactive (P/Q) power at PCC bus in per unit system, the expression can be carried out as follows.

$$P = v_d i_d + v_q i_q \tag{2}$$
$$Q = v_q i_d - v_d i_q \tag{3}$$

Due to the PCC reference frame, $v_d = V_{pcc}$ and $v_q = 0$, then the expressions can be rewritten as:

$$P = V_{pcc} i_d \tag{4}$$
$$Q = -V_{pcc} i_q \tag{5}$$

From above expression, it shows that the real power control required negative feedback control loop and reactive power control needs positive feedback.

For inner control, the algorithm is concluded from circuit analysis. On dq-reference frame, the dynamic equation can be written as follows.

$$L\frac{di_d}{dt} = -Ri_d + \underbrace{e_d - V_{pcc} + L\omega i_q}_{u_d} \tag{6}$$

$$L\frac{di_q}{dt} = -Ri_q + \underbrace{e_q - L\omega i_d}_{u_q}, \tag{7}$$

where e_d and e_q are the VSC terminal voltage's dq-components. The equations above can explain the structure of the current control, where the current PI controllers' outputs are u_d and u_q, respectively. In order to generate e_d and e_q order. cross-coupling term $-\omega L i_q$ and feedforward term V_{PCC} are added to u_d to generate e_d. Simailarly, cross-coupling term $\omega L i_d$ is added to u_q to generate e_q.

In the end, the terminal voltage dq-components are sent into the Inverse Park Transformation to generate the control reference signal with the estimated phase angle, ωt. Table. III presents all the gains for PI controllers in the testbed.

TABLE III: Parameters of the controller

Item	Value	Item	Value
$K_{p,P}$	0.4	$K_{i,P}$	45
$K_{p,Q}$	0.4	$K_{i,Q}$	40
K_{p,i_d}	0.4758	K_{i,i_d}	3.2655
K_{p,i_q}	4	K_{i,i_q}	15

D. Steady State Analysis

To study the operation condition of the grid-following VSC, the steady state analysis is performed based on power flow via constrained optimization formulated within YALMIP. Solver used is IPOPT.

With PQ control implemented, the PCC bus power follows the reference at steady state. The equality constraints can be formulated as follows.

```
Constraints= [P_ref == P; Q_ref == Q];
```

Between PCC bus and grid voltage source, the only unknown variables are the V_{pcc} and θ_{pcc}, and they are introduced as symbolic decision variables (sdpvars). To grab real and reactive power, the transmission line current phasor, $\bar{I}_g$ is carried out as follows.

$$\bar{I}_g = \frac{\bar{V}_{pcc} - \bar{V}_g}{R_g + jX_g} \tag{8}$$

The complex power at PCC bus can be obtained from the following expression.

$$S_{pcc} = \bar{V}_{pcc}\bar{I}_g^* \tag{9}$$

In the end, take the real and imaginary parts of the complex power into the constraints for objective solving. The formulated problem is shown below.

```
Vpcc = sdpvar(1);
theta = sdpvar(1);
assign(Vpcc,1);
assign(theta,0);

vpcc = Vpcc*exp(1i*theta);
Vg = 1;
i = (vpcc-Vg)/(Rg+1i*Xg);

S = vpcc*conj(i);
P = real(S); Q = imag(S);
```

To solve the objective within constraints, the values of V_{pcc} and θ_{pcc} are obtained. Furthermore, by changing the system parameters, such as grid voltage magnitude and transmission line impedance, the stability of the system can be examined under weak grid and voltage dip condition [4].

III. Case Study

In the case study, the SOGI-PLL performance is first examined to track a single-phase AC voltage signal under magnitude increase, frequency dip, and phase angle jump. Then, the instantaneous power with FFT analysis is presented. Next, the simulation result will show PQ regulation capability of the control. Finally, the testbed is simulated under weak grid, voltage dip, and frequency dip conditions with steady state limit approaching via YALMIP.

A. SOGI-PLL Demonstration

The SOGI-PLL in Fig. 2 is implemented in MATLAB/Simulink individual to test its performance. The input signal is a single-phase AC voltage signal with no noise. The following events are designed for presenting [10].

- *Event 1:* Input magnitude increase
- *Event 2:* Input frequency drop
- *Event 3:* Input phase angle jump
- *Event 4:* Combined dynamic event

Figure. 5 presents dynamic response in Event 1. At 1 second, the input voltage has a magnitude step change from 1 to 1.5 per unit. Upper plot shows the input AC voltage signal, the lower plot shows the estimated voltage magnitude from SOGI-PLL can track the reference change.

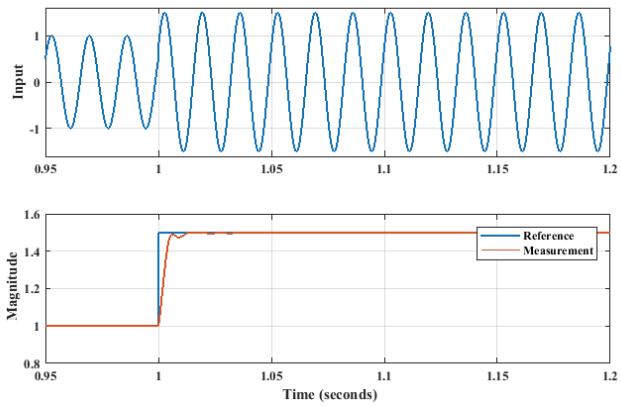

Fig. 5: Magnitude change of the SOGI-PLL.

In Event 2, the input voltage signal experiences a frequency dip from 60 Hz to 50 Hz at 1 second. Figure. 6 shows the input signal and estimated frequency.

In Figure. 7, the estimated phase angle is compared to the reference signal while the input signal has a phase angle jump

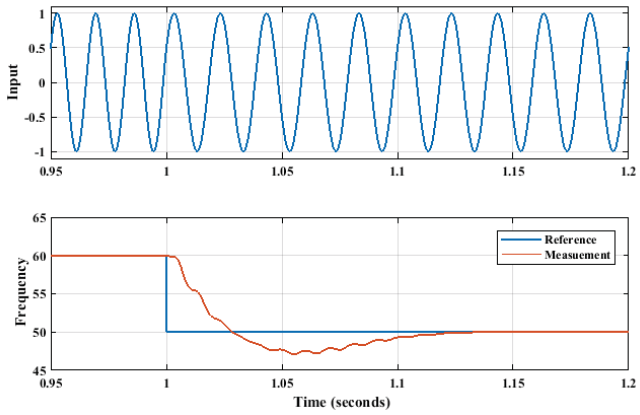

Fig. 6: Frequency change of the SOGI-PLL.

from 0 degree to 30 degree at 1 second. The upper plot shows the rotating phase angle (in rad) tracking and the lower plots shows the static phase angle tracking (in degree).

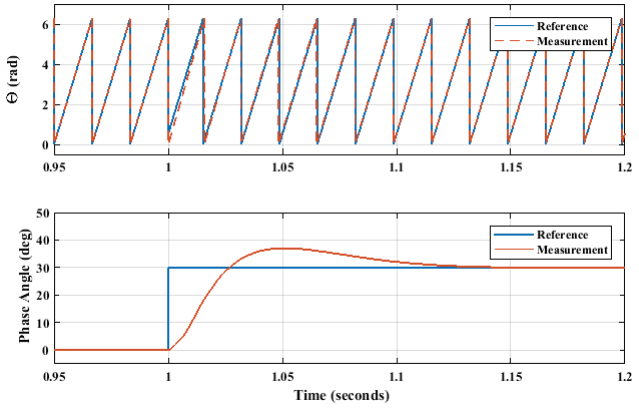

Fig. 7: Phase change of the SOGI-PLL (θ= wt).

For Event 4, multiple changes are applied on the input signal for testing SOGI-PLL's performance. At 1 second, the input signal gets a magnitude drop from 1 to 0.8 pu, a frequency increase from 60 Hz to 70 Hz, and a phase jump from 0 to 15 degree. Figure. 8 shows the comparison between input and estimated v_α, as well as, v_β, which is 90 degrees behind.

B. Double frequency ripple of instantaneous power

In time domain, the instantaneous power in the single-phase AC system will include a DC component and an AC ripple. The ripple frequency is double of the fundamental frequency. Assume the instantaneous voltage ($v(t)$) and current ($i(t)$) are expressed as follows.

$$v(t) = \sqrt{2}V_{rms}\cos(\omega t) \tag{10}$$

$$i(t) = \sqrt{2}I_{rms}\cos(\omega t + \phi) \tag{11}$$

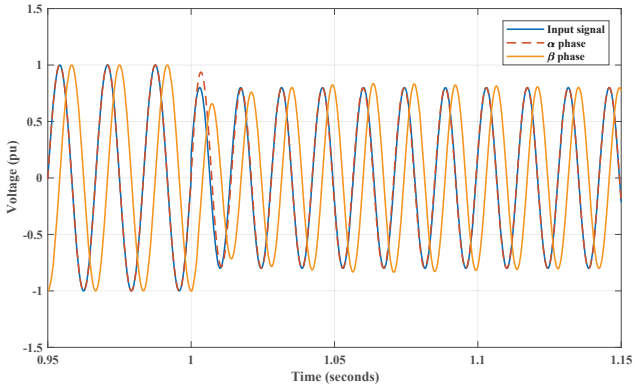

Fig. 8: Multiple changes of the SOGI-PLL.

The instantaneous power ($p(t)$) can be derived as shown below.

$$p(t) = v(t)i(t) \tag{12}$$

$$= \underbrace{V_{rms}I_{rms}\cos(\phi)}_{\text{DC Component}} + \underbrace{V_{rms}I_{rms}\cos(2\omega t + \phi)}_{\text{Double frequency component}} \tag{13}$$

Fig. 9 shows the collected instantaneous power measurement from the simulation testbed. The fundamental frequency of the system is 60 Hz. The ripple frequency is 120 Hz.

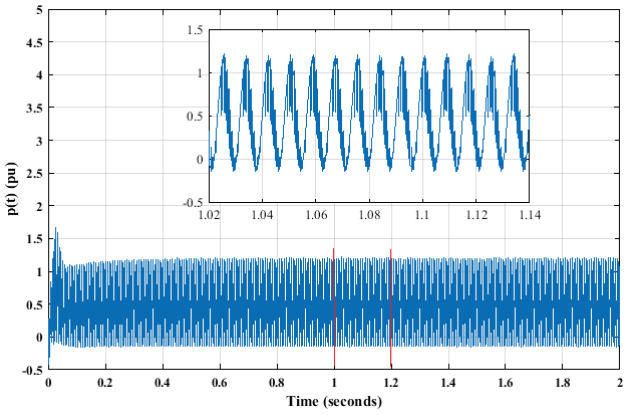

Fig. 9: Instantaneous power of the PCC bus.

To verify, the data is analyzed with Fast Fourier Transform. Fig. 10 clearly presents there is a DC components at a magnitude of 0.5 and a 120 Hz dominated component at a magnitude of 0.58.

C. Power regulation capability

With PQ control algorithm implemented, the VSC is operated in grid-following mode. To examine the PQ control function, step changes are applied on reference signals, P_{ref} and Q_{ref}. Initially, the real power is 0.5 pu and the reactive power is 0.3 pu. At 1.5 second, P_{ref} increases from 0.5 to 0.8 pu. And at 2 second, Q_{ref} decreases from 0.3 to 0.1 pu. Fig. 11. shows the power regulation results. The red curves are the reference signals and blue curves are the measurements.

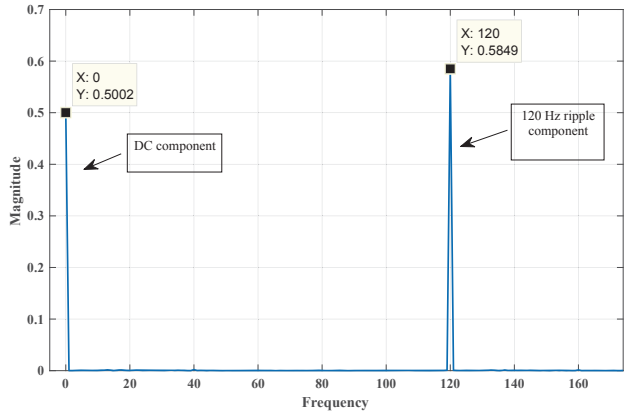

Fig. 10: FFT analysis of instantaneous power.

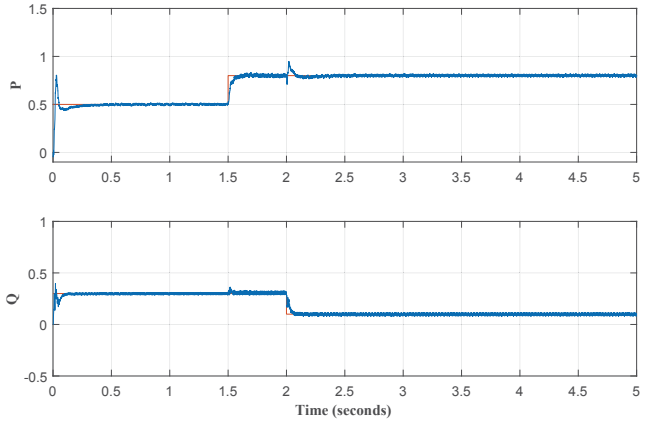

Fig. 11: Real power, reactive power and its step.

D. Weak grid condition

As the transmission line extending, the line reactance increases and the grid becomes weaker. In the case study, the line impedance is gradually increased until system collapses. Before moving on to the simulation, steady-state power flow analysis is performed. From the YALMIP solving, it is found that the marginal reactance causes unstable condition is 1.85 pu. However, the simulation testbed hires the detailed IGBT switches. Due to the harmonics, the real system limit is slightly lower.

The designed dynamic events are shown as follows. The measurement of the PCC bus real power is shown in the Fig. 12.

- Event 1: Line impedance increases from 1.6 to 1.7 pu
- Event 2: Line impedance increases from 1.6 to 1.8 pu
- Event 3: Line impedance increases from 1.6 to 1.9 pu

From Fig. 12, the real power measurement shows that system is stable in Event 1; system is still stable but weakened in Event 2 due to longer settling time; system suddenly lost stability in Event 3. The true marginal reactance for weak grid connection in the testbed is examined to be 1.81 pu, which is closed to the steady state analysis limit approaching.

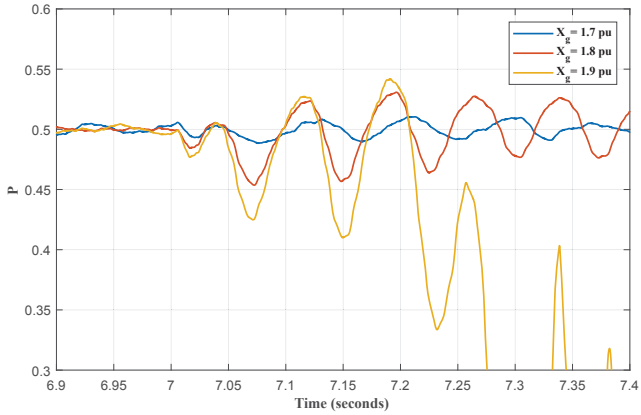

Fig. 12: Measurements of PCC bus real power under different line reactance.

E. Grid voltage dip

In large power system, the voltage dip could appear when there is a fault somewhere not too far away from the measurement bus. For the relatively small system in this paper, the single-phase grid voltage dip is designed to emulate the fault condition.

Same as previous case study, the voltage dip limit is obtained from YALMIP solving. According to the approaching results, it finds that the minimum grid voltage magnitude to maintain the stability is 0.32 pu. From the simulation testbed, the observed marginal grid voltage magnitude is 0.37 pu, which is relatively accurate.

The dynamic events are designed as follows.

- Event 1: voltage dip from 0.5 pu to 0.39 pu
- Event 2: voltage dip from 0.5 pu to 0.37 pu
- Event 3: voltage dip from 0.5 pu to 0.35 pu

The time-domain measurement of grid voltage and PCC bus voltage after a filter are shown in Fig. 13, and the real power measurement to indicate the system stability is shown in Fig. 14.

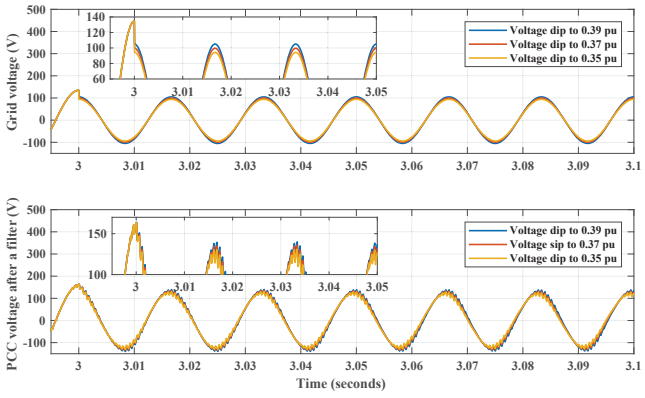

Fig. 13: Grid voltage and PCC bus voltage after a filter

From Fig. 14, it can tell when the grid voltage magnitude dips across the marginal voltage can cause the instability issue.

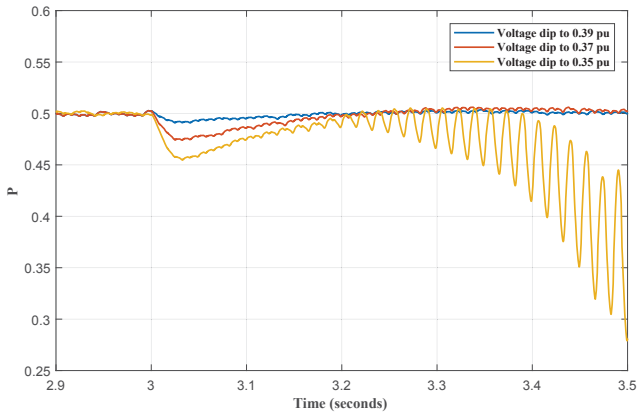

Fig. 14: Measurements of PCC bus under different grid voltage dip

F. Grid frequency dip

Similar to previous case study, instead of dipping grid voltage magnitude, the grid voltage frequency dip is examined. From the simulation results, it is found that the marginal frequency for system to maintain stable status is 41 Hz. The comparison dynamic events are designed as follows.

- Event 1: Grid voltage frequency decreases from 60 Hz to 46 Hz
- Event 2: Grid voltage frequency decreases from 60 Hz to 40 Hz
- Event 3: Grid voltage frequency decreases from 60 Hz to 40 Hz

The frequency estimated from SOGI-PLL is presented on top of Fig. 15, and the real power measurement is shown on the bottom. As shown, for frequency dips, the SOGI-PLL can always track the change. However, when the frequency dips to 41 Hz, an oscillation lasts for 1 second before the system went back to stable. Further, when frequency dips across the margin to 40 Hz, the system collapsed.

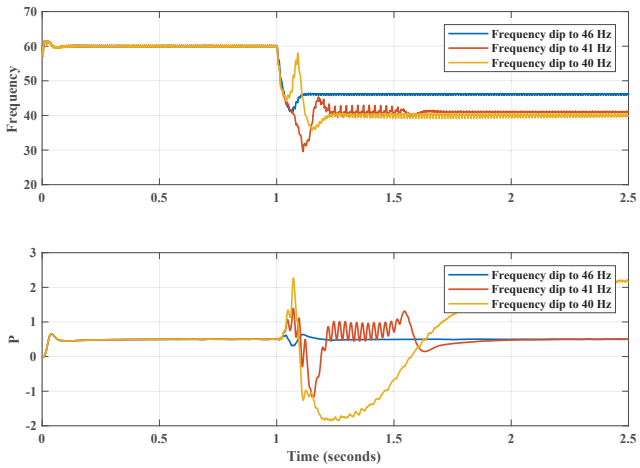

Fig. 15: Frequency dip

IV. Conclusion

In this paper, a Simulink/SimPowerSystem EMT testbed of single-phase VSC in grid-following mode is presented. The VSC type is detailed IGBT switch-based. The control algorithm implementation including SOGI-based PLL and $\alpha\beta$-components extraction are discussed in detail. Several case studies on SOGI-PLL, instantaneous power analysis, controller capability, and system operation limits are demonstrated.

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