Fast Model Predictive Control Algorithms for Fast-Switching Modular Multilevel Converters

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Abstract

For high-power/voltage systems, particularly for high-voltage direct current (HVDC), one of the most potential converter topologies is the modular mutlilevel converter (MMC). Model predictive control (MPC) is one of the switching methods studied in the literature for MMC to simultaneously achieve the three challenging objectives of 1) following the reference of the current waveform requested by upper-level control, 2) mitigating on circulating current, and 3) regulating capacitor voltages of submodules. Since the MPC models proposed in the literature suffers from high computation burdens making the algorithm not applicable to high-frequency switching MMCs, a binary integer programming based MPC has been proposed in this paper to optimize this multi-objective problem with minimum computing effort. The main contribution of the algorithms proposed in this paper is to significantly reduce the computation expenses by cutting the searching space from millions of feasible solutions to the incredibly low number of "4", while taking care of the three objectives of MMC control. The performance of the proposed method is evaluated via simulation in MATLAB SimPowerSystems.

Keywords: High Switching Frequency, Model Predictive Control, Modular Multilevel Converter.

1. Introduction

Modular Multilevel Converter (MMC) is reported in the literature as the most promising topology proposed for Voltage Source Converters (VSC) due to its salient characteristics such as scalability and modularity [1–7].

Simultaneous regulation of submodule capacitor voltages and elemination/minimization of the circulating current flowing through three phases of the converter is still one of the technical challenges associated with MMC application due to their mutual effects. Circulating current, in fact, not only is a function of the capacitor voltages of the submodules turned on at each time step, but also determines how the capacitor

voltages of the same submodules change until the next switching time step arrives, which may lower the efficiency of the converter and cause more ripples in the capacitor voltages if it is not well suppressed. However, it should be noted that the circulating current is a useful mean to balance the energies between all six arms in situations where some energy unbalance are caused by asymmetric operations and fault situations and tolerances of the components [8].

The method proposed in [1] compares all possible switching combinations for the MMC switches in one bridge for their predicted performance one step ahead. This method requires significant computing effort. At each time step with the step size defined by the switching frequency, e.g. 100 μs for 10 kHz, the solution must be sought. For a 5-level MMC, there are 8 submodules in each bridge. Among the eight submodules, four submodules should be turned on to keep the dc-link voltage constant. Therefore, the number of the combination is $C_8^4 = 70$. The algorithm needs to check 70 possible on/off sequences and find the best one. For a 13-level MMC, C_{24}^{12}, or 2.7 million combinations should be checked. For a 16-level MMC, 155 million combinations should be checked.

In the authors' previous paper [9], a one-step model predictive control has been proposed. The proposed method aims to track the ac reference currents and eliminate the circulating currents. Based on the two objectives, the optimal upper-arm voltage and lower-arm voltage for a MMC bridge can be found. Based on the desired voltage level, capacitor voltages are sorted in order. When the arm current is positive, the capacitors with lowest voltages will be switched on to get charged. When the arm current is negative, the capacitors with the highest voltages will be switched off to get discharged. This method requires only sorting algorithms, which makes it efficient for MMCs with a large number of submodules.

The disadvantage of the above algorithm is its omission of the dc-voltage constraint. The number of submodules to be switched on is required to be fixed in PWM scheme and the MPC scheme proposed in [1]. In order to take this constraint into account, a mathematical programming problem is formulated and solved using heuristic way. In many papers, commercial solvers such as CPLEX are employed to solve MIP problems [10, 11]. However, for this power electronics application, it is not feasible to employ a commercial solver. Firstly, the switching scheme will be programmed in a chip. It is not possible to have a commercial solver on a chip. Secondly, commercial solvers use general methods to solve optimization problems. In many cases, CPLEX has convergence issues due to its adoption of enumeration. For special optimization problems, a specific solving method will achieve much faster solving speed than a commercial solver.

In this paper, the mathematical model of MPC-based (n-1)-level MMC, which has n submodules at each arm, is proposed in order to track ac reference current, mitigate circulating current and to keep capacitor

voltage nominal subject to selection of exactly n submodules to be trigged at each arm. The multi-objective optimization problem is then reformulated to a new model and the weighting sum method is employed to merge the objectives. To solve such problem, two algorithms are represented to seek the optimal solution for switching pattern. The first search algorithm design remarkably reduces the size of feasible solution to n instead of C_{2n}^{n}, but the simulation results shows that it has serious drawbacks in satisfying the objectives of MPC, which has led the authors to an alternative algorithm for better performance while maintaining the computation advantages. The second algorithm is developed by applying a relaxation on the constraint of number of switched-on submodules and increases the size of the feasible set to n^2, which introduces additional computation burden compared the first algorithm especially for high values of n. However, it is proved in this paper that this size can be cut down to 4 if appropriate weighting factors are selected and checking just 4 of the solutions is enough to find the optimal solution. This paper is focused on the lower-level switching control design where the upper-level control signals are assumed to be given as reference values. The efficiency of the algorithms are finally tested via simulations in MATLAB SimPowerSystems.

The following sections of the paper are organized as follows: Section 2 presents the MMC mathematical model. Section 3 presents the MPC strategy and the binary integer programming solving algorithms. Section 4 reports the simulation results of MPC based switching schemes. Section 5 concludes the paper.

2. Mathematical Model of the MMC

2.1. System Topology

Fig. 1 shows a simplified scheme for a three-phase MMC. At each phase of A, B, or C, there are two groups of switches on upper and lower arms. Fig. 2 shows the structure of each arm of a 7-level MMC. Each arm consists of 6 submodules (SM) each of which has two IGBT switches and a capacitor. There are two inductors in each phase in order to provide current control and limit the fault currents.The voltage of each submodule is either equal to its capacitor voltage $V_{C,i}$ or zero depending on the states of the two switches. Table 1 lists the submodule output voltage. The on/off states of the two switches of a submodule are always opposite to each other. The total voltage of one arm will be the sum of its submodules' voltages and the voltage across the inductor.

2.2. MMC Circuit Analysis

The ac current of each phase (e.g., phase a) can be represented by the corresponding upper-arm (i_{up}) and lower-arm (i_{low}) currents, as below:

$$i_a = i_{up,a} - i_{low,a} \tag{1}$$

Hereafter, the subscripts "a", "b", and "c" standing for three phases will be ignored for simplicity of the equations. One of the objectives of the MPC control to mitigating the circulating currents in the arms. The total current in an upper-arm or lower-arm has three components: $\frac{1}{3}$ of the dc current i_{dc}, a component related to the ac current, and the circulating current i_z. The following equations represent the relationship of the currents:

$$i_{up} = \frac{i}{2} + \frac{i_{dc}}{3} + i_z \tag{2}$$

$$i_{low} = -\frac{i}{2} + \frac{i_{dc}}{3} + i_z \tag{3}$$

Although i_z only circulates through the converter legs and does not affect the AC side current, the circulating current has adverse impact on the voltage ripples of the capacitors, converter loss, and rating of power electronic components of MMC. Hence, the circulating current must be mitigated.

Based on the above mentioned equations (2) and (3), the circulating current flowing through each phase can be expressed in terms of its upper-arm and lower-arm currents as well as and converter dc-side current as follows:

$$i_z = \frac{i_{up} + i_{low}}{2} - \frac{i_{dc}}{3} \tag{4}$$

According to Fig. 1, the dynamic behavior of the each phase of MMC is determined by the following equations:

$$v_{up} = \frac{V_{dc}}{2} - l\frac{di_{up}}{dt} - Ri - L\frac{di}{dt} - v_s \tag{5}$$

$$v_{low} = \frac{V_{dc}}{2} - l\frac{di_{low}}{dt} + Ri + L\frac{di}{dt} + v_s \tag{6}$$

where v_s denotes the grid voltage.

Subtracting (6) from (5) leads to

$$v_{low} - v_{up} = l\frac{di}{dt} + 2Ri + 2L\frac{di}{dt} + 2v_s \tag{7}$$

while adding the two equations results in

$$v_{low} + v_{up} = V_{dc} - 2l\frac{di_z}{dt} \tag{8}$$

The dynamic of capacitor voltage of the submodule i is also described by

$$C\frac{dv_{Cj}}{dt} = i_{up}u_j \qquad \forall j \in [1, n] \tag{9}$$

$$C\frac{dv_{Cj}}{dt} = i_{low}u_j \qquad \forall j \in [n+1, 2n] \tag{10}$$

where $u_j = 1$ if submodule j is active, and $u_j = 0$ otherwise.

2.3. Discrete Model of MMC

According to (7) and its Euler's approximation of the current derivative, the next step value for ac-side current can be written as

$$i(t+T_s) = \frac{1}{K'}\left(\frac{v_{low}(t+T_s) - v_{up}(t+T_s)}{2} - v_s(t+T_s) + \frac{L'}{T_s}i(t)\right) \tag{11}$$

where T_s is an adequately small sampling time step, $L' = L + l/2$, and $K' = R + L'/T_s$. The time indices (t) and $(t+T_s)$ denotes the measured values at current time and the predicted values for the next time step, respectively. As the sampling frequency is assumed to be large enough compared to grid frequency, the predicted value of grid voltage $v_s(t+T_s)$ can be replaced by its measured value $v_s(t)$. $v_{up}(t+T_s)$ and $v_{low}(t+T_s)$ are the predicted upper-arm and lower-arm voltages which are defined as

$$v_{up}(t+Ts) = \sum_{j=1}^{n} v_{Cj}(t+Ts)u_j \tag{12}$$

$$v_{low}(t+Ts) = \sum_{j=n+1}^{2n} v_{Cj}(t+Ts)u_j \tag{13}$$

where, according to (9)-(10),

$$v_{Cj}(t+Ts) = v_{Cj}(t) + \left(\frac{T_s i_{up}(t)}{C}\right)u_j \qquad \forall j \in [1, n] \tag{14}$$

$$v_{Cj}(t+Ts) = v_{Cj}(t) + \left(\frac{T_s i_{low}(t)}{C}\right)u_j \qquad \forall j \in [n+1, 2n] \tag{15}$$

The discrete description of (8) leads to the following equation to represent the next-step circulating current:

$$i_z(t+T_s) = \frac{T_s}{2l}\left(V_{dc} - v_{low}(t+T_s) - v_{up}(t+T_s)\right) + i_z(t) \tag{16}$$

3. Model Predictive Control

3.1. MPC Multiobjective Problem

According to the mathematical model of the MMC, an MPC strategy is proposed in this section. The proposed MPC strategy seeks the best switching sequences of u_i to control ac-side current, capacitor voltage, and circulating current simultaneously.

Three objectives have been defined for MMC control in the literature[1]:

i to track the ac-side current (i) of all phases to their reference values (i_{ref})

ii to mitigate the circulating current i_z flowing between the converter legs, and

iii to regulate all the capacitor voltages on their nominal value (V_{dc}/n)

Assuming that the capacitor voltages are kept very close to their nominal value (V_{dc}/n), one constraint on total number of switched-on submodules is defined. Indeed, half of the submodules on each phase must be switched on and the other half must be off, all the time. The multi-objective optimization problem is illustrated as below,

$$\begin{aligned}
&\text{min} && |i_{ref} - i(t+T_s)| \\
&\text{min} && |i_z(t+T_s)| \\
&\text{min} && \left| V_{C_i}(t+T_s) - \frac{V_{dc}}{n} \right| \\
&\text{over:} && \{u_1, u_2, ..., u_n\} \\
&\text{subject to:} && (11) - (16) \\
& && \sum_{i=1}^{2n} u_i = n
\end{aligned} \tag{17}$$

3.2. Optimization Alternative 1

3.2.1. Problem Reformulation

Let us define $(\cdot)^*(t+T_s)$ to be the ideal value of corresponding variable for the next time step. By replacing the variables in (11) by their ideal values implying *exact AC current tracking*,

$$i^*(t+T_s) = i_{ref} = \frac{1}{K'}\left(\frac{v^*_{low}(t+T_s) - v^*_{up}(t+T_s)}{2} - v_s(t+T_s) + \frac{L'}{T_s}i(t)\right) \tag{18}$$

which leads to the following relation between v^*_{low} and v^*_{up}:

$$v^*_{low}(t+T_s) - v^*_{up}(t+T_s) = 2K' i_{ref}(t+T_s) + 2v_s(t) - \frac{2L'}{T_s} i(t) \tag{19}$$

Likewise, for zero circulating current in the bridges, replacing the ideal value of i_z in (16) leads to

$$i^*_z(t+T_s) = \frac{T_s}{2l}\left(V_{dc} - v^*_{low}(t+T_s) - v^*_{up}(t+T_s)\right) + i_z(t) = 0 \tag{20}$$

which determines another relation between $Vlow*$ and $Vup*$ which is proposed below:

$$v^*_{low}(t+T_s) + v^*_{up}(t+T_s) = V_{dc} + \frac{2l}{T_s} i_z(t) \tag{21}$$

The variables $v^*_{low}(t+T_s)$ and $v^*_{up}(t+T_s)$ are derived from (19) and (21) as follows:

$$v^*_{low}(t+T_s) = \left(\frac{V_{dc}}{2} + \frac{l}{T_s} i_z(t)\right) + \left(K' i_{ref}(t+T_s) + v_s(t) - \frac{L'}{T_s} i(t)\right) \tag{22}$$

$$v^*_{up}(t+T_s) = \left(\frac{V_{dc}}{2} + \frac{l}{T_s} i_z(t)\right) - \left(K' i_{ref}(t+T_s) + v_s(t) - \frac{L'}{T_s} i(t)\right) \tag{23}$$

where V_{dc} is assumed to be constant. Let the variables Δv_{low}, Δv_{up}, and Δi denote the deviation of the corresponding variables from their ideal values, defined as below:

$$\Delta v_{low} = v^*_{low} - v_{low} \tag{24}$$

$$\Delta v_{up} = v^*_{up} - v_{up} \tag{25}$$

$$\Delta i = i_{ref} - i(t+T_s) \tag{26}$$

Subtraction of (11) from (18) gives an explanation of the first objective function (ac current deviation) in terms of v^*_{up} and v^*_{low}, as follows:

$$\Delta i = \frac{1}{2K'}\left(\Delta v_{low}(t+T_s) - \Delta v_{up}(t+T_s)\right) \tag{27}$$

The explanation of the second objective function (circulating current) in terms of v^*_{up} and v^*_{low} is also derived

by subtracting (20) from (16):

$$i_z(t+T_s) = \frac{T_s}{2l}\left(\Delta v_{low}(t+T_s) + \Delta v_{up}(t+T_s)\right) \tag{28}$$

Hence, (27) and (28) can be applied to (17).

$$\min_U \quad f_1(U) = \frac{1}{2K'}\left|\Delta v_{low}(t+T_s) - \Delta v_{up}(t+T_s)\right| \tag{29}$$

$$\min_U \quad f_2(U) = \frac{T_s}{2l}\left|\Delta v_{low}(t+T_s) + \Delta v_{up}(t+T_s)\right| \tag{30}$$

$$\min_U \quad f_3(U) = \sum_{i=1}^{2n}\left|V_{C_i}(t+T_s) - \frac{V_{dc}}{n}\right| \tag{31}$$

$$\text{subject to:} \quad (11)-(16), (22)-(25)$$

$$\sum_{i=1}^{2n} u_i = n \tag{32}$$

$$U = [u_1, u_2, ..., u_{2n}] : u_k \in \{0,1\}\ \forall k \in [1, 2n]$$

Applying weighted sum method to the optimization problem (17) leads to the following formulation, which is called P_1 hereafter:

$$\min_U \quad f_4(U) = \frac{\lambda}{2K'}\left|\Delta v_{low}(t+T_s) - \Delta v_{up}(t+T_s)\right| + \frac{\lambda_z T_s}{2l}\left|\Delta v_{low}(t+T_s) + \Delta v_{up}(t+T_s)\right| \tag{33}$$

$$\min_U \quad f_3(U) = \sum_{i=1}^{2n}\left|V_{C_i}(t+T_s) - \frac{V_{dc}}{n}\right| \tag{34}$$

$$\text{subject to:} \quad (11)-(16), (22)-(25)$$

$$\sum_{i=1}^{2n} u_i = n \tag{35}$$

$$U = [u_1, u_2, ..., u_{2n}] : u_k \in \{0,1\}\ \forall k \in [1, 2n]$$

where the first objective is derived by applying the weighted sum method to the objective functions $f_1(U)$ and $f_2(U)$ with coefficients λ and λ_z, respectively. The weighted sum method with equal coefficient is also employed to merge the third objective function to a single objective function for capacitor voltage deviation.

3.2.2. Solution Algorithm 1

The approach proposed in this paper to solve the multi-objective optimization problem P_1 includes three steps. First, the function corresponding to the capacitor voltage deviation (34) sorts the submodules to be switched on. Next, the priorities defined are used to form the feasible solution sets considering the constraint (35). Finally, the objective function (33) determines the best switching pattern based on the feasible solution sets determined previously.

Step 1. This step minimizes the second objective function (34) by sorting the submodules on both the upper and lower arm. According to (14), the direction of i_{up} defines whether the capacitor voltages of the upper-arm submodules are subjected to increase or decrease. Since the capacitor of a switched-on submodule gets charged when $i_{up} > 0$, the algorithm prefers to select the submodules with least capacitor voltages. Thus they are sorted in the ascending order. Likewise, the submodules are sorted in the descending order if $i_{up} < 0$. Let the vector $V_{C_{up}}^{sort} = [V_{C_1}^{sort}, ..., V_{C_n}^{sort}]$ denote the submodule voltages on the upper-arm after sorting. The algorithm applies the same logic to sort the submodules on the lower-arm to define the vector $V_{C_{low}}^{sort} = [V_{C_{n+1}}^{sort}, ..., V_{C_{2n}}^{sort}]$.

Step 2. Having the submodules sorted based on their capacitor voltages, the algorithm calculates the cumulative sum vectors of the components of $V_{C_{up}}^{sort}$ and $V_{C_{low}}^{sort}$. The sets of cumulative sum values are denoted as $V_{C_{up}}^{sum}$ and $V_{C_{low}}^{sum}$ are defined as below:

$$V_{C_{up}}^{sum} = \{\alpha_k : k = 0, 1, ..., n\} \tag{36}$$

$$V_{C_{low}}^{sum} = \{\beta_k : k = 0, 1, ..., n\} \tag{37}$$

where

$$\alpha_0 = \beta_0 = 0$$

$$\alpha_k = \sum_{i=1}^{k} V_{C_i}^{sort} \qquad \forall k \in [1, n]$$

$$\beta_k = \sum_{i=n+1}^{n+k} V_{C_i}^{sort} \qquad \forall k \in [1, n]$$

To make sure that the number of the submodules that switched on is n, the sum of the subscripts of α and β should add up to n. Fig. 3-a describes all n feasible solutions $U \in S$ where each $\leftrightarrow$ represents one feasible solution.

Step 3. The size of feasible set is now remarkably lower than that introduced in [1]. The algorithm then compares the objective function (33) for all feasible solutions to find the optimal solution $U^* = \text{argmin} f_4(U) : U \in S$. If more than one $U \in S$ minimizes the function f_4, the one returning less value for f_3 is the final solution.

3.3. Optimization Alternative 2

3.3.1. A Relaxation to the Problem P_1

The simulation results of the algorithm and optimization problem P_1 illustrates that the constraint (35) has an adverse impact on the circulating current. The constraint, in fact, restricts the algorithm from selecting the most appropriate solution to mitigate the circulating current.

In this section, a modified version of the optimization problem P_1 is solved to overcome this problem. The first modification is to eliminate the constraint (35) from the optimization problem. Therefore, the algorithm is able to switch on as many submodules as required to reach v^*_{up} and v^*_{low}. Second, the weighting factors λ and λ_z are set on the values $2K'$ and $\frac{2l}{T_s}$ respectively. Having the first and second modifications applied to P_1, it is changed to the following format which will be called P_2 hereafter:

$$\min_{U} \quad f_5(U) = |\Delta v_{low}(t+T_s) - \Delta v_{up}(t+T_s)| + |\Delta v_{low}(t+T_s) + \Delta v_{up}(t+T_s)| \tag{38}$$

$$\min_{U} \quad f_3(U) = \sum_{i=1}^{2n} \left| V_{C_i}(t+T_s) - \frac{V_{dc}}{n} \right| \tag{39}$$

$$\text{subject to:} \quad (11)-(16), (22)-(25)$$

$$U = [u_1, u_2, ..., u_{2n}] : u_k \in \{0,1\}\ \forall_{k\in[1,2n]}$$

3.3.2. Solution Algorithm 2

Similar to the previous algorithm, Solution Algorithm 2 solves the multiobjective problem P_2 in three steps.

Step 1. The first step is to sort the submodules according to their capacitor voltages and the sign of upper-arm and lower-arm currents, which is described in the first step of the algorithm 1. $V^{sort}_{C_{low}}$ and $V^{sort}_{C_{low}}$ are the outputs of step 1.

Step 2. Having the submodules sorted, sets of $V^{sum}_{C_{up}}$ and $V^{sum}_{C_{low}}$ are defined using (36)-(37). The feasible solution set S includes the switching sequences associated with any $(\alpha_i, \beta_j) \in V^{sum}_{C_{up}} \times V_{C_{up}}$. Fig. 3-b

represents the combinations of v_{up} and v_{low} which form feasible solutions of the optimization problem P_2, where each $\leftrightarrow$ represents one feasible solution. The total number of the feasible sets are n^2. Although the searching space is significantly reduced compared to the number of the sets examined in [1], it still needs significant computational efforts to compare the resulting objective f_5 for each feasible set and find the optimal set, especially for the converters with large number of submodules *e.g.* $n = 400$. The reasoning provided in the next step makes the solution much more efficient.

Step 3. According to proof stated in Appendix, if $v^*_{up} \in [\alpha_i, \alpha_{i+1})$ and $v^*_{low} \in [\beta_j, \beta_{j+1})$, the objective function f_5 is needed to be calculated for just four (v_{up}, v_{low}) combinations belonging to

$$\{(\alpha_i, \beta_j), (\alpha_{i+1}, \beta_j), (\alpha_i, \beta_{j+1}), (\alpha_{i+1}, \beta_{j+1})$$

to determine the optimal switching pattern. In case more than one $U \in S'$ minimizes the function $f_5(U)$, the one returning lower value for $f_3(U)$ is the final solution.

Remark 1: The first two objective functions in (17) are translated in terms of $v_{up} - v^*_{up}$ and $v_{low} - v^*_{low}$ in (29) and (30), which cannot be completely fulfilled due to the discrete nature of the problem. The sorting algorithm proposed for capacitor voltage regulation also makes it worse due to remarkably decreasing the number of possible solution. Elimination of the constraint (35) is indeed a trick to compensate the effect of voltage sorting algorithm on the number of possible solutions. Consider a case where $i_{up} > 0$ and $i_{low} > 0$. In such a case, the sorting algorithm puts the submodules with lowest capacitor voltages in priority on both upper and lower arms. Most likely, selecting exactly n submodules with lowest voltages will result in $v_{up} + v_{low} \ll V_{dc} - 2l\frac{di_z}{dt}$. Relaxing the constraint (35) enables the algorithm to consider more submodules to be switched on, which might help the algorithm to fulfill $v_{up} + v_{low} \approx V_{dc} - 2l\frac{di_z}{dt}$. The simulation results provided below demonstrates that the total number of switched-on submodules on upper and lower arms $(\sum_{i=1}^{n} u_i)$ is equal to either n most of the time, which results in a good regulation of dc link voltage.

Remark 2: Both switching methods are summarized as **Algorithm 1** and **Algorithm 2** below.

4. Case Study

4.1. Study System

This section evaluates the performance of an MMC system of Fig. 1. The case study is performed against a back-to-back MMC systems with no common capacitor connected to dc link, in order to evaluate the effects of switching on dc link voltage as well. Both MPC strategies proposed in this paper (Algorithm

Algorithm 1 With constraints on number of active submodules.

for all phases a,b,c **do**
Collect measurements of capacitor voltages, arm currents, and dc current.
Calculate v^*_{low} and v^*_{up} using (22)-(23).
if $i_{up} > 0$ **then**
Sort $\{V_{C_i} | i = 1, \cdots, n\}$ in ascending order and call the vector $V^{sorted}_{C_{up}}$.
else
Sort $\{V_{C_i} | i = 1, \cdots, n\}$ in descending order and call the vector $V^{sorted}_{C_{up}}$.
end if
if $i_{low} > 0$ **then**
Sort $\{V_{C_i} | i = n+1, \cdots, 2n\}$ in ascending order and call the vector $V^{sorted}_{C_{low}}$.
else
Sort $\{V_{C_i} | i = n+1, \cdots, 2n\}$ in descending order and call the vector $V^{sorted}_{C_{low}}$.
end if
Create the vectors $V^{sum}_{C_{up}}$ and $V^{sum}_{C_{low}}$ as defined in (36)-(37).
for any $k \in 0, 1, \cdots, n$ **do**
Calculate $A_k = f_5(O(\alpha_k, \beta_{n-k}))$ using (38).
Calculate $B_k = f_3(O(\alpha_k, \beta_{n-k}))$ using (39).
end for
Find the minimum value of A_k and save the corresponding sequences of $O(\alpha_k, \beta_{n-k})$ in the set U^*.
Find the minimum value of B_k for the sequences belonging to U^* and report the corresponding sequence as the final solution.
end for

Algorithm 2 No constraints on number of active submodules.

for all phases a,b,c **do**
Collect measurements of capacitor voltages, arm currents, and dc current.
Calculate v^*_{low} and v^*_{up} using (22)-(23).
if $i_{up} > 0$ **then**
Sort $\{V_{C_i} | i = 1, \cdots, n\}$ in ascending order and call the vector $V^{sorted}_{C_{up}}$.
else
Sort $\{V_{C_i} | i = 1, \cdots, n\}$ in descending order and call the vector $V^{sorted}_{C_{up}}$.
end if
if $i_{low} > 0$ **then**
Sort $\{V_{C_i} | i = n+1, \cdots, 2n\}$ in ascending order and call the vector $V^{sorted}_{C_{low}}$.
else
Sort $\{V_{C_i} | i = n+1, \cdots, 2n\}$ in descending order and call the vector $V^{sorted}_{C_{low}}$.
end if
Create the vectors $V^{sum}_{C_{up}}$ and $V^{sum}_{C_{low}}$ as defined in (36)-(37).
Define i such that $\alpha_i \leq v^*_{up} < \alpha_{i+1}$.
Define j such that $\beta_j \leq v^*_{low} < \beta_{j+1}$.
Let $k = 0$.
for any $(\alpha, \beta) \in \{\alpha_i, \alpha_{i+1}\} \times \{\beta_j, \beta_{j+1}\}$ **do**
Calculate $A_k = f_5(O(\alpha, \beta))$ using (38).
Calculate $B_k = f_3(O(\alpha, \beta))$ using (39).
Let $k = k + 1$.
end for
Find the minimum value of A_k and save the corresponding sequences of $O(\alpha, \beta)$ in the set U^*.
Find the minimum value of B_k for the sequences belonging to U^* and report the corresponding sequence as the final solution.
end for

1 and Algorithm 2) are applied on this system to compare the performance. In practice, an MMC-HVDC can have a large number of submodules in each arm. In order to simplify the simulation study without loss of generality, a 7-level MMC is considered and simulated in MATLAB/Simpowersystem environment. The system parameters are given in Table 2. The ac-side voltage is expected to be 52 kV(line-to-line, peak value), and the reference of the ac-side current is 300 A in phase with the ac voltage. For Algorithm 1, the weighting factors λ and λ_z are selected equal to one another *e.g.* $\lambda = \lambda_z = 1$. Increasing λ_z in respect to λ improves the circulating current minimization, but would have adverse effects on ac current tracking.

4.2. Simulation Result

Figs. 4 and 5 present the comparison of N_{up}, N_{low} and the total number of switched-on submodules for both cases. The switching scheme based on Algorithm 1 results in total six submodules to be switched on at all time. However, for Algorithm 2, due to the relaxation, the total number of submodules to be switched on can be also 7 or 5. However, according to the percentage of the total number of switched-on submodules for Algorithm 2 based on the simulation results which is illustrated in Fig. 6, in 75% percent of the switching sequences the total number of the submodules turned on is equal to 6. This value is equal to 5 and 7 in 11% of the incidents, each.

Fig. 7 presents the circulating current in phase a. In Algorithm 1, the circulating current is not well mitigated due to the constraint on total number of switched-on submodules. In contrary, the algorithm 2 has more freedom to seek the best solution for circulation current suppression.

Fig. 8 presents the ac currents for the three cases. Both algorithms lead to an appropriate switching scheme from current tracking point of view. The ac current waveforms completely follow the sinusoidal current reference with correct amplitude and phase.

As shown in Fig. 9, where the first submodule's capacitor voltage is depicted for both algorithms, Algorithm 1 results in a $\pm 10\%$ ripple on capacitor voltage mostly because of its unsuccessful mitigation of the circulating current. In contrast, the capacitor voltage of the case simulated by Algorithm 2 has just $\pm 1\%$ ripple which proves the efficiency of this algorithm for this objective as well.

Fig. 10 also shows the dc voltage link voltage throughout the simulation time for Algorithm 2. According to the results shown in Fig. 10 the dc link voltage varies between 0.9 and 1.1 pu during simulation. However, the histogram of the dc link voltage signal illustrated in Fig. 11 resembles a normal distribution with a mean value and a standard deviation equal to $\mu = 0.9972pu$ and $\sigma = 0.0344pu$, respectively. That is, the dc link voltage is well regulated since the mean value is sufficiently close to 1 pu and the standard deviation is less the negligible value of 3.5%.

5. Conclusion

In this paper, binary integer programming based MPC strategies with significantly less computing effort has been proposed to control the ac currents, keep the capacitor voltages nominal, and mitigate the circulating currents. The algorithm also determines which submodules to be switched on/off for the next time step according to the corresponding upper/lower current. The proposed algorithms use sorting to find the feasible solution sets. These feasible solution sets are then compared for their objective values. The performance of the proposed methods are evaluated via simulation in MATLAB SimPowerSystems. The proposed MPC schemed are compared for their control effort and performance. It is found that MPC based schemes are capable to achieve better ac current tracking and circulating current elimination.

APPENDIX

In this section, it is proved that the optimal solution of P_2 cannot lie on any feasible solution other than (α_i, β_j),(α_{i+1}, β_j),(α_i, β_{j+1}), and $(\alpha_{i+1}, \beta_{j+1})$ if $v^*_{up} \in [\alpha_i, \alpha_{i+1})$ and $v^*_{low} \in [\beta_j, \beta_{j+1})$.

Let us define $V_C^{sum} = V_{C_{up}}^{sum} \times V_{C_{low}}^{sum}$ and the function $O : V_C^{sum} \to \mathbf{U}$ mapping any $(\alpha_i, \beta_j) \in V_C^{sum}$ to its corresponding switching $U_{i,j} \in \mathbf{U}$ such that $U_{i,j} = O(\alpha_i, \beta_j)$. Fig. 12 illustrates a geometric representation of the feasible set S assuming that $v^*_{up} \in [\alpha_i, \alpha_{i+1})$ and $v^*_{low} \in [\beta_j, \beta_{j+1})$. The subset $S' \subset S$ is also defined as

$$S' = \{O(\alpha_i, \beta_j), O(\alpha_{i+1}, \beta_j), O(\alpha_i, \beta_{j+1}), O(\alpha_{i+1}, \beta_{j+1})\}$$

which includes the switching sequences corresponding to the points 1-4 shown in Fig. 12.

Claim: The optimal solution in feasible set S certainly belongs to the subset S', that is, $\{\min f_5(U) : U \in S'\} = \{\min f_5(U) : U \in S\}$.

Proof: For any feasible solution $U_{k,l} = O(\alpha_k, \beta_l)$, the objective function (38) equals to

$$f_5(U_{k,l}) = 2 \times \max\left\{|\alpha_k - v^*_{up}|, |\beta_k - v^*_{low}|\right\} \tag{40}$$

Having the *Region 1* in Fig. 12 defined as $R_1 = \{(k,l)|k \leq i, l \leq j\}$ spanning the feasible solution subset

$S_1 = \{U_{k,l} | k \leq i, l \leq j\}$, we have

$$\left|\alpha_i - v^*_{up}\right| \leq \left|\alpha_k - v^*_{up}\right|$$
$$\left|\beta_j - v^*_{low}\right| \leq \left|\beta_l - v^*_{low}\right|$$

for any $(k, l) \in R_1$, which leads to

$$\min\{f_5(U) : U \in S_1\} = f_5(U_{i,j}) \tag{41}$$

regarding (40). Similarly, the subsets

$$S_2 = \{U_{k,l} | k \leq i, l > j + 1\}$$
$$S_3 = \{U_{k,l} | k > i + 1, l > j + 1\}$$
$$S_4 = \{U_{k,l} | k > i + 1, l \leq j\}$$

are respectively associated with the *Regions 2-4* in Fig. 12. Extending the justification discussed for *Region 1* to the *Regions 2-4* illustrates that

$$\min\{f_5(U) : U \in S_2\} = f_5(U_{i,j+1}) \tag{42}$$
$$\min\{f_5(U) : U \in S_3\} = f_5(U_{i+1,j+1}) \tag{43}$$
$$\min\{f_5(U) : U \in S_4\} = f_5(U_{i+1,j}). \tag{44}$$

According to (41)-(44), the optimal solution definitely lies on one of the solutions belonging to the subset S', and the claim is proved. Thus, the algorithm suffices to compare the value of $f_5(U)$ for the feasible solutions belonging to S' to seek the optimal solution.

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Table of Tables

Table 1: Submodule Voltage.

State	$S1$	$S2$	V_{SM}
$0(inactive)$	OFF	ON	0
$1(active)$	ON	OFF	V_C

Table 2: Case Study Parameters.

Quantity	Value	
MMC nominal power	50	MVA
Nominal DC voltage V_{dc}	60	kV
Submodule capacitor C_{sm}	2500	μF
Carrier signal frequency f	2.5	kHz
Output current reference I_{ref}	300	A
R	0.03	Ω
L	5	mH
l	3	mH
Sampling period T_s	25	μs

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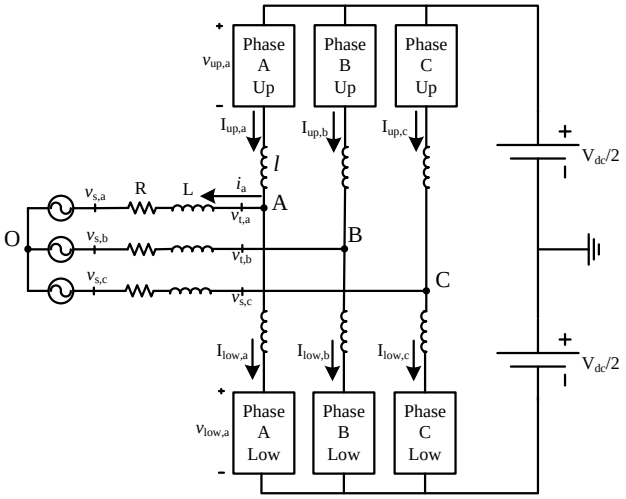


Figure 1: Simplified scheme of a multilevel modular converter.

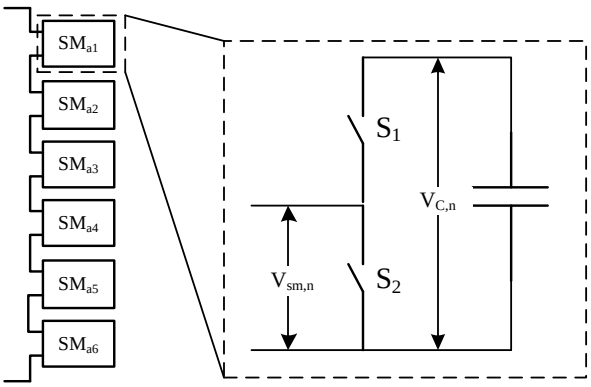


Figure 2: The structure of MMC submodules.

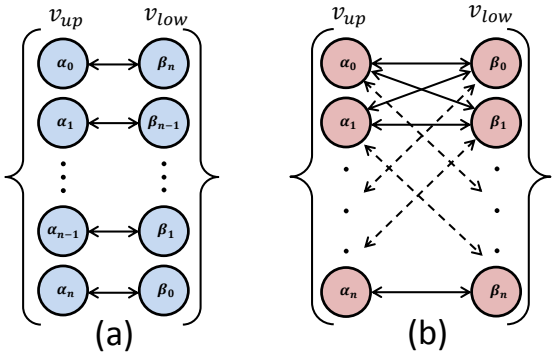


Figure 3: (a) Feasible solution set of P_1 according to Algorithm 1, (b) Feasible solution set of P_2 according to Algorithm 2.

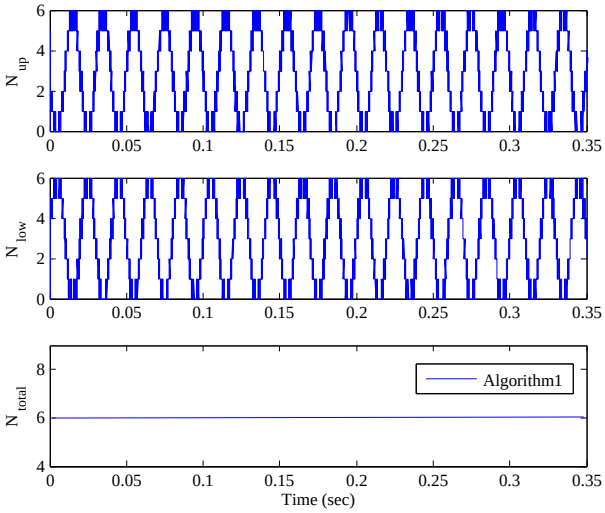


Figure 4: Number of active submodules in the upper arm, the lower arms and the entire bridge for Algorithm 1.

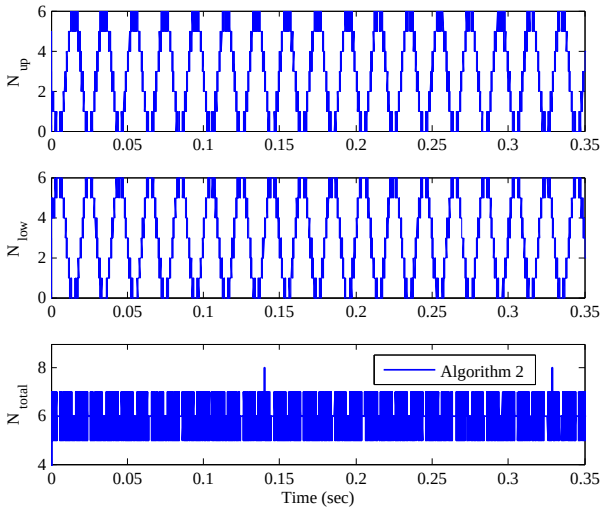


Figure 5: Number of active submodules in the upper arm, the lower arms and the entire bridge for Algorithm 2.

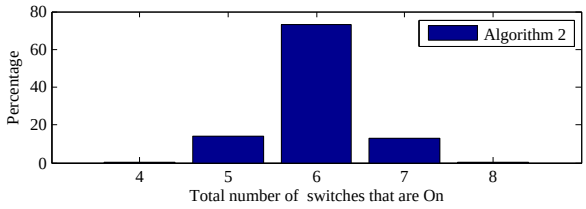


Figure 6: Histogram of the number of active submodules for Algorithm 2, obtained from simulations.

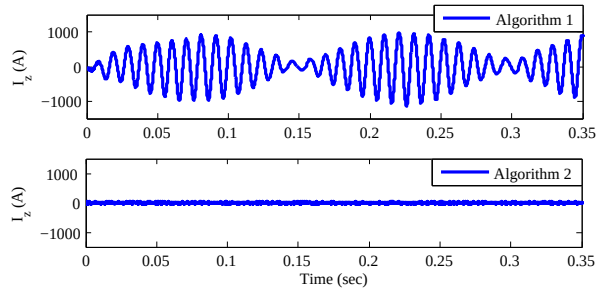


Figure 7: Circulating current in different switching methods.

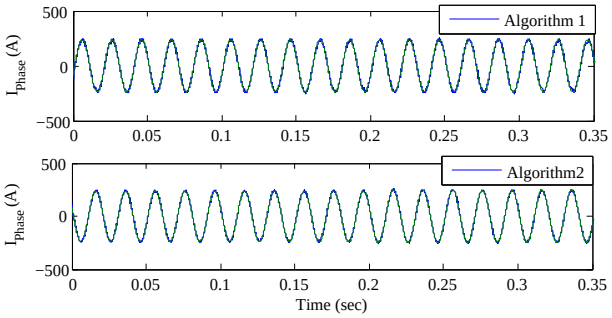


Figure 8: Output phase current in different switching methods.

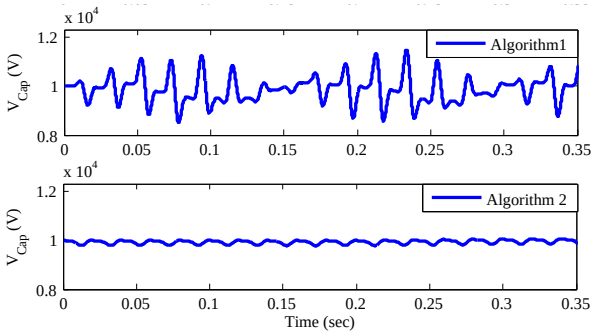


Figure 9: Capacitor voltage in different switching methods.

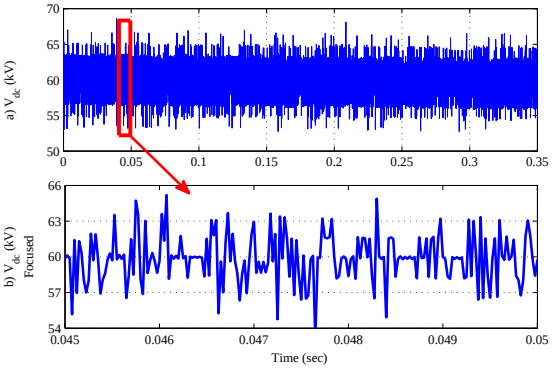


Figure 10: DC link voltage signal for switching Algorithm 2.

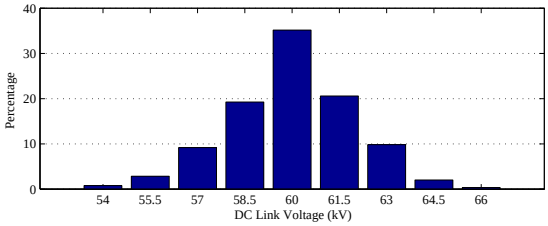
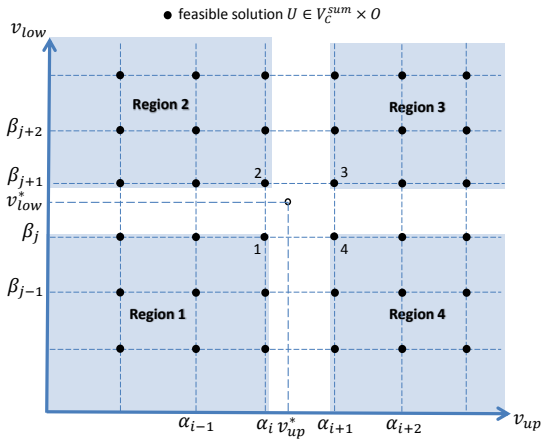


Figure 11: Histogram of DC link voltage values for Algorithm 2, obtained from simulation results.



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